

Digital backends

DBBC and Fila10G

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Overview

- Digital Backends
- Operating modes: DDC / PFB / DSC
- DBBC generations example
- FILA10G and FILA40G network translators

General Functionality VLBI Schematic Block



Requirements 'around' the backend area

- Demand for an always **wider bandwidth**: receivers, data transport and correlators play their role, but backend should not be the bottle-neck
- New fast and powerful **technologies** are every day available
- New **connectivity** through a fast network is every day increasing
- Improvement of the **phase stability** in the entire signal path is a must
- **Obsolescence** and difficulties in the analogue systems maintenance
- **New** radiotelescopes need new equipment
- More **flexibility** in number of bands and/or polarization
- More **reliability**

The need for a fully digital VLBI backend

- ‘Digital Radio’ technology become familiar within new telecommunication developments requiring frequency conversion
- Technology was ready for the VLBI needed performance
- A new generation of stations without any VLBI terminal could also greatly benefit from a new development



Why more Digital?

- Digital is completely deterministic
- Precise and predictable modelling/performance
- Amplitude/Phase characteristics stable as sampling clock
- Wider, flatter pass-band, well matched between systems
- No dispersion and group delay distortion across the pass-band

Why more Digital? (cont)

- Reduced closure errors for a better calibration
- Much more compact implementation
- One hardware platform for many architectures and functions
- Cost effective for high performance multi-channel systems
- Process numerical with all the related implications
- RFI Mitigation can be greatly simplified

How to take this into consideration?

A general worldwide trend is to use more digital and less analog for predictability, repeatability, precision, etc.

This means to try and perform the

conversion from

ANALOG to DIGITAL

anticipated in the processing time as much as possible

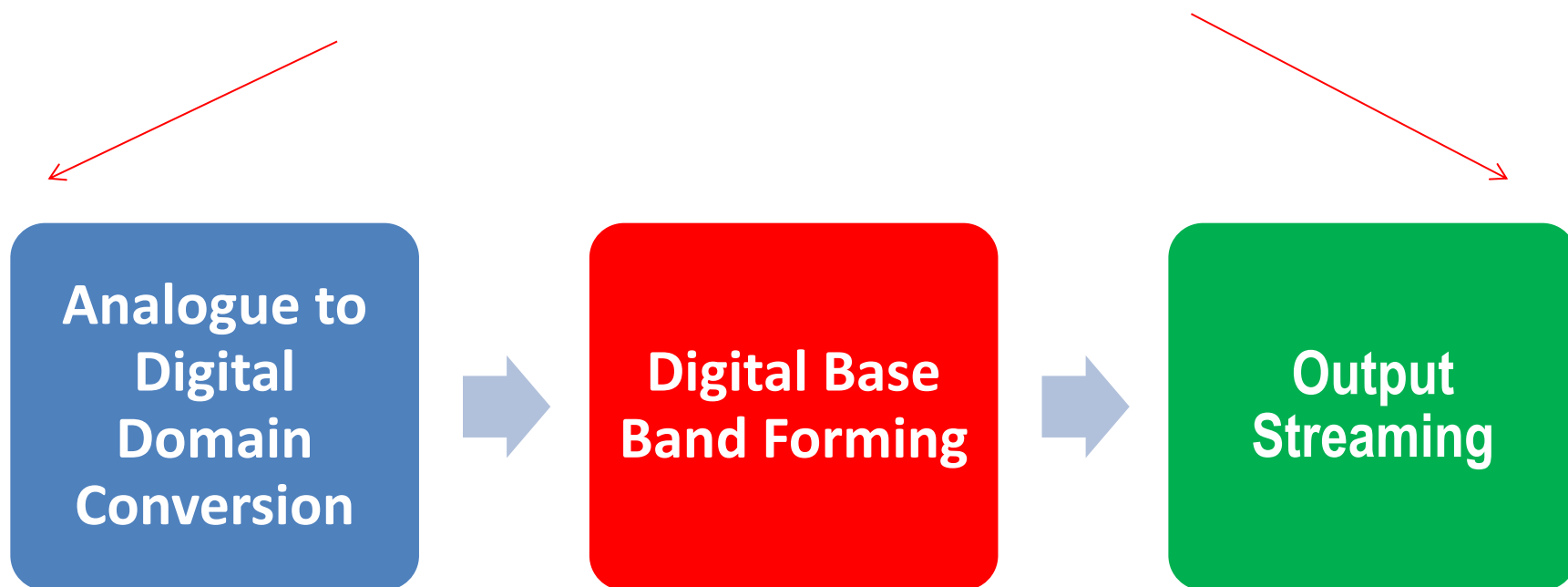
and to use

DIGITAL SIGNAL PROCESS

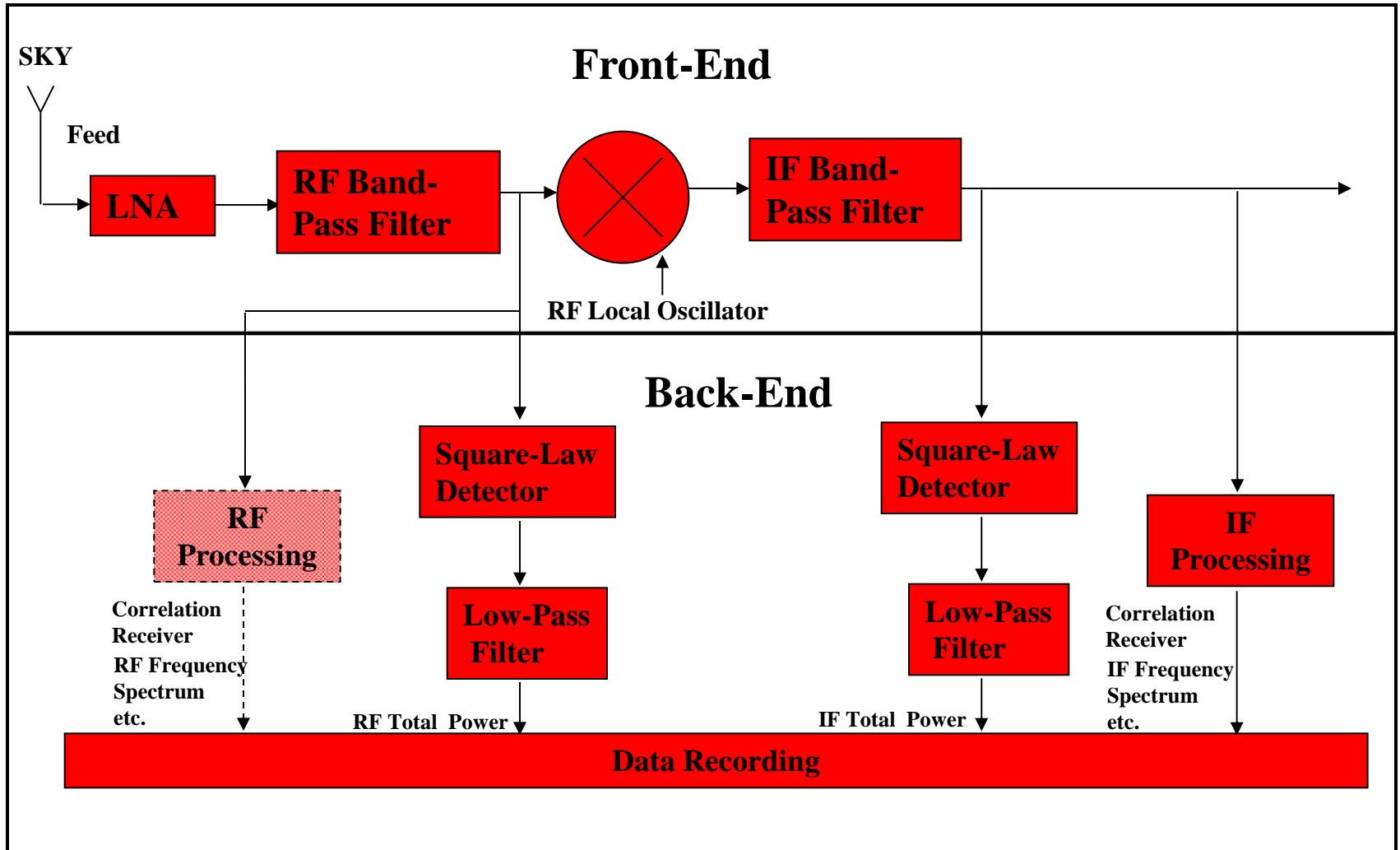


General Functionality

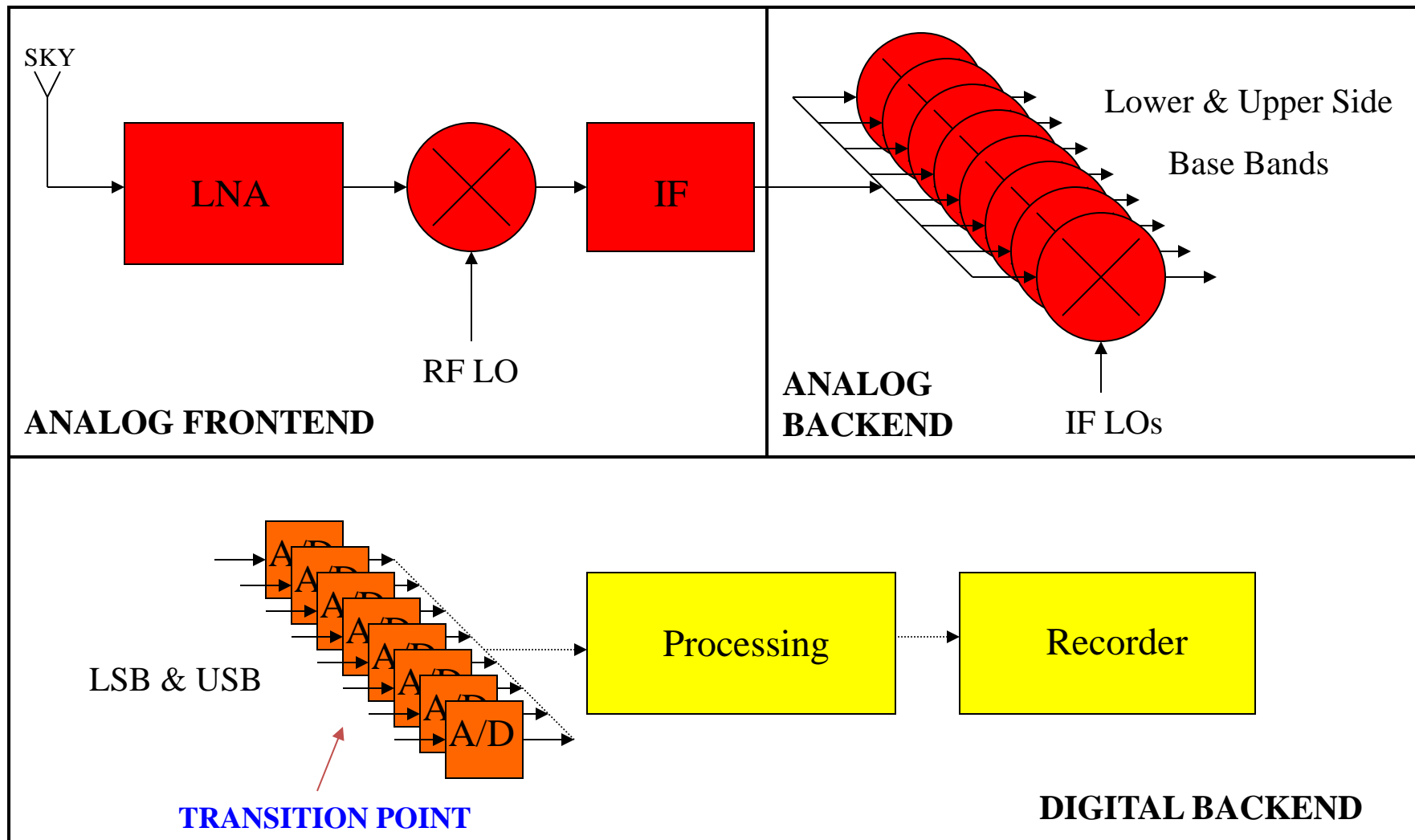
Backend Schematic Block



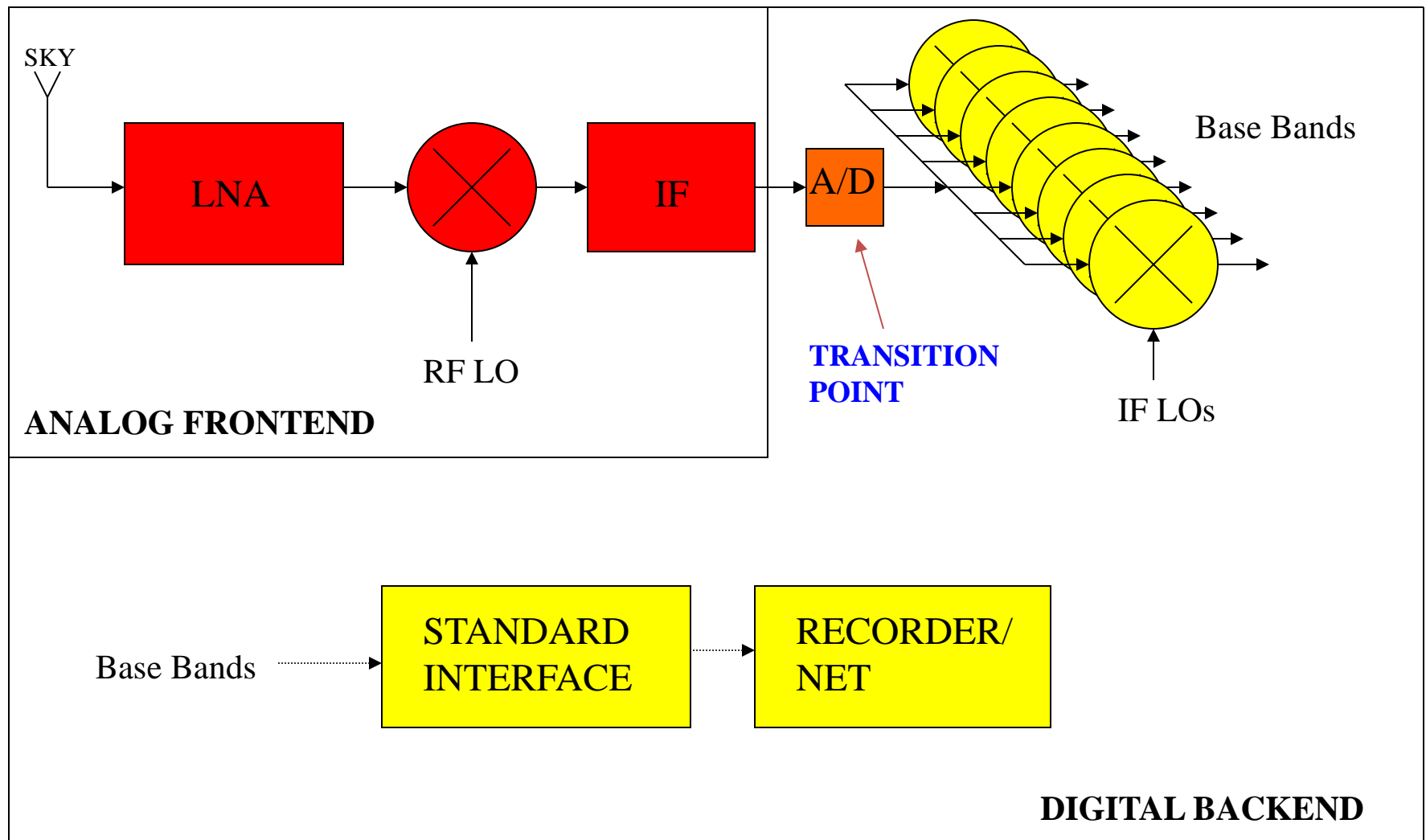
Receiving and Acquisition Chain in the Radiotelescope



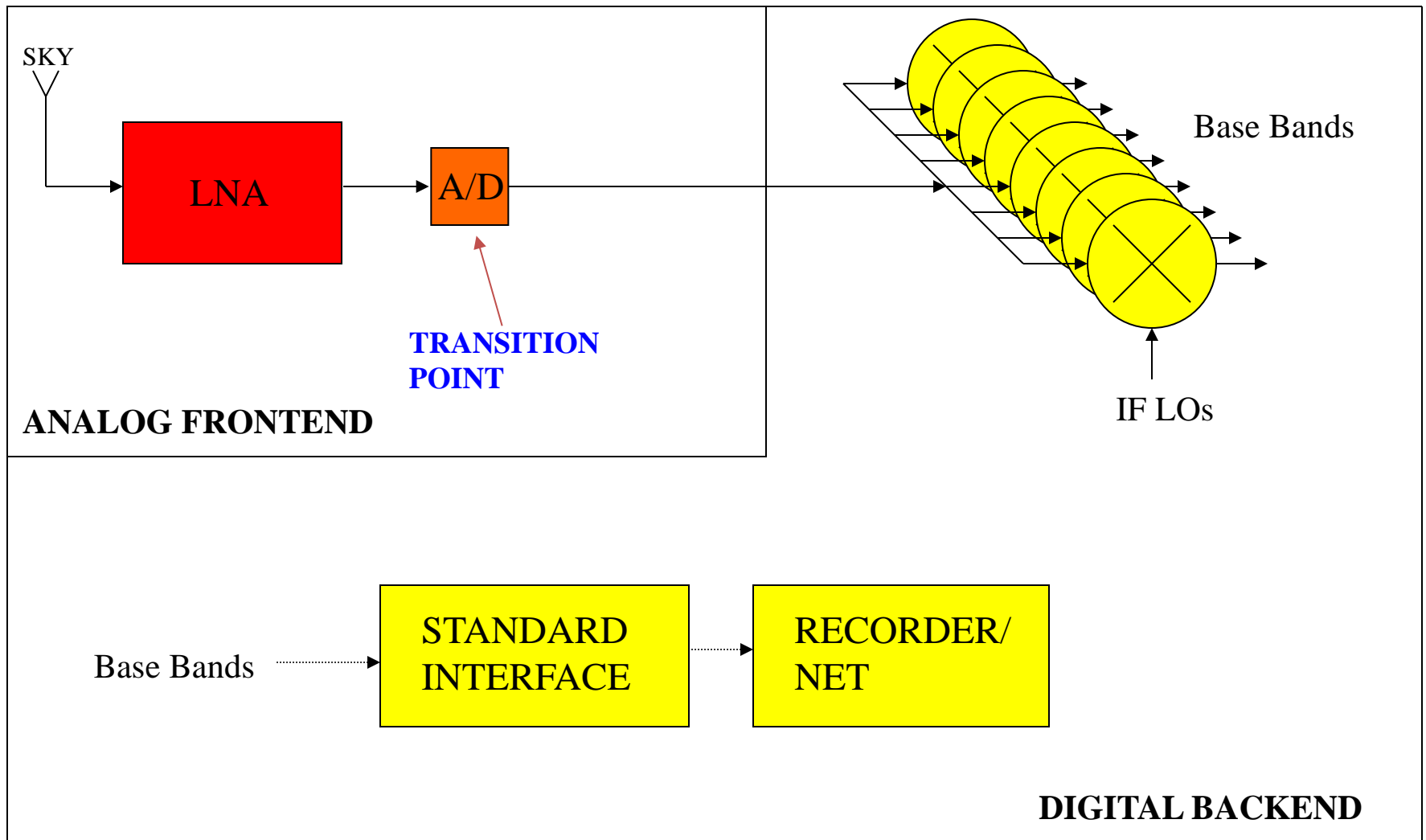
Front- and Back-End Multichannel Chain



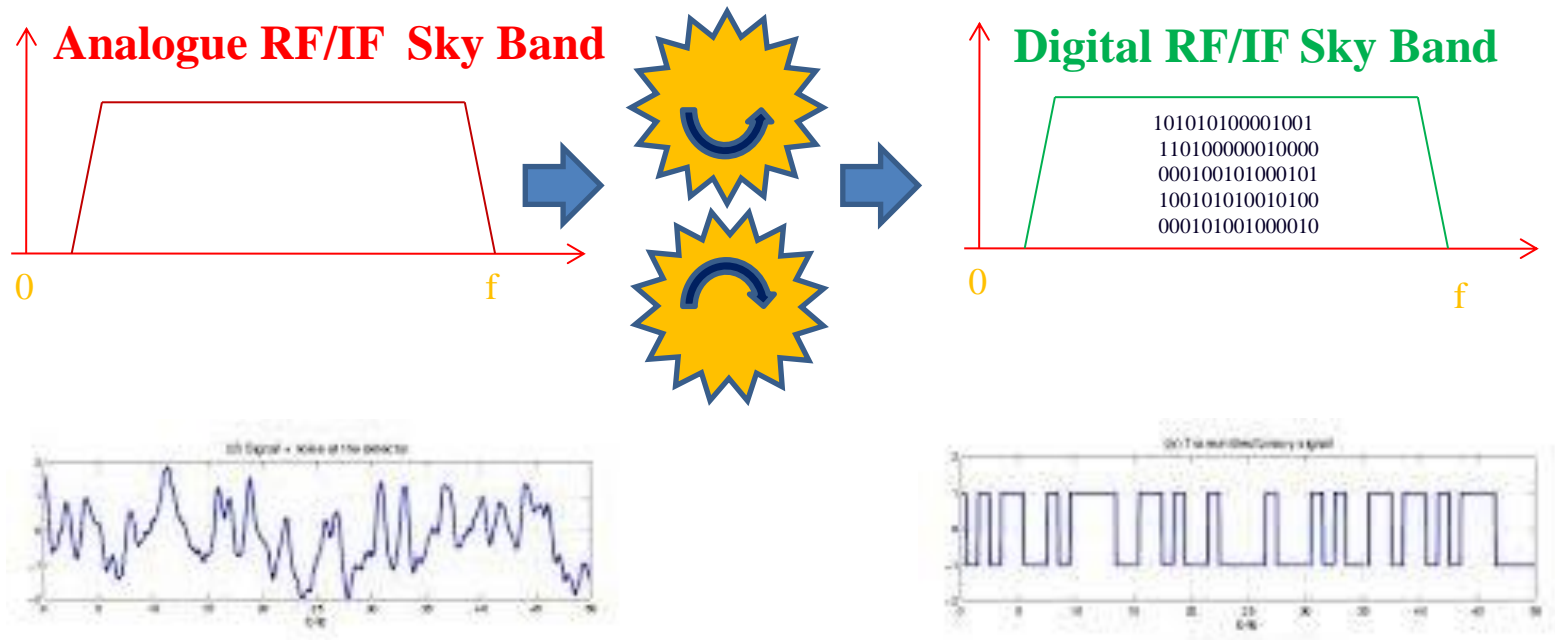
Advanced Front- and Backend Chain



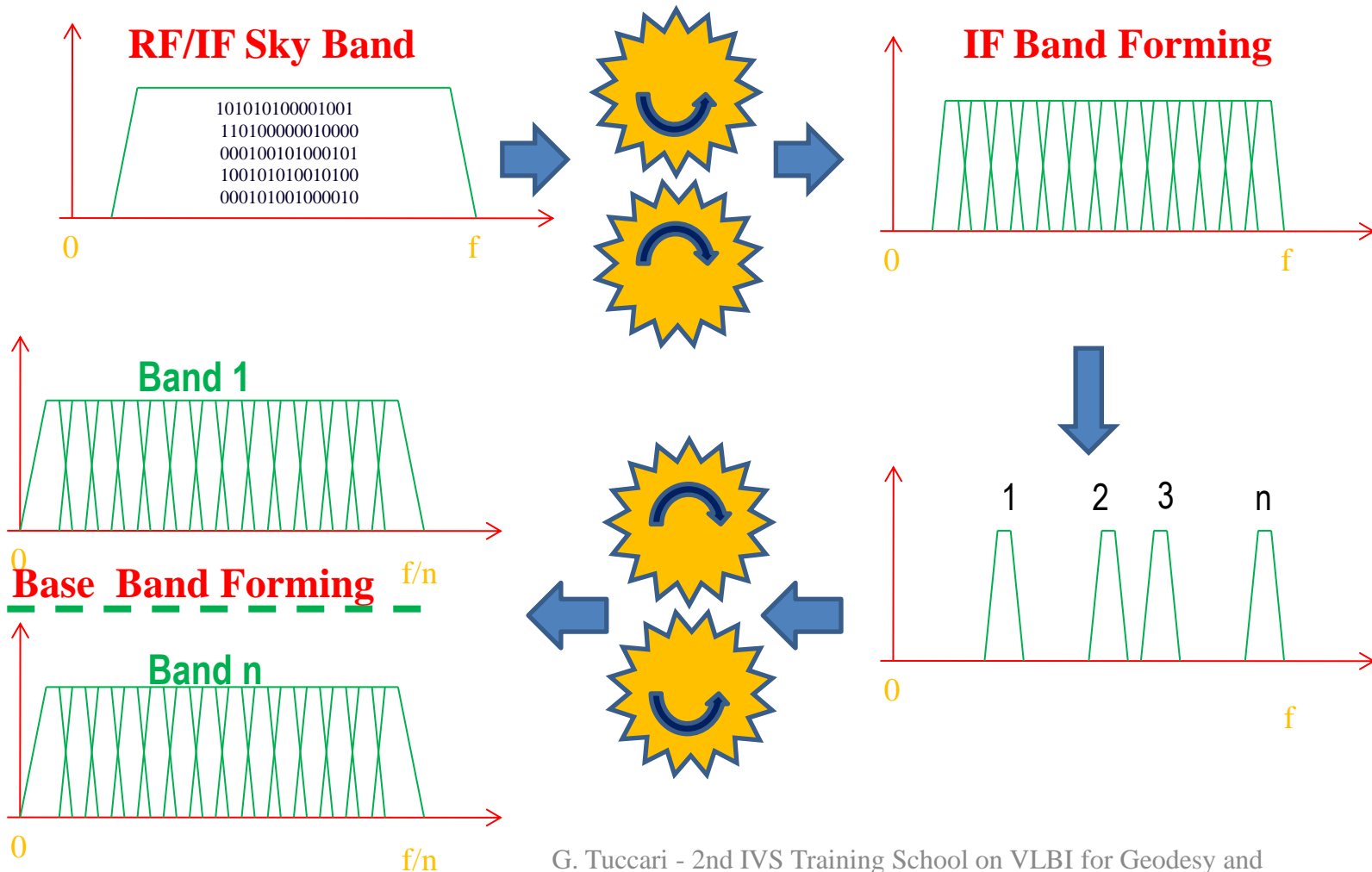
Advanced Front- and Backend Chain



Analogue to Digital Domain Conversion

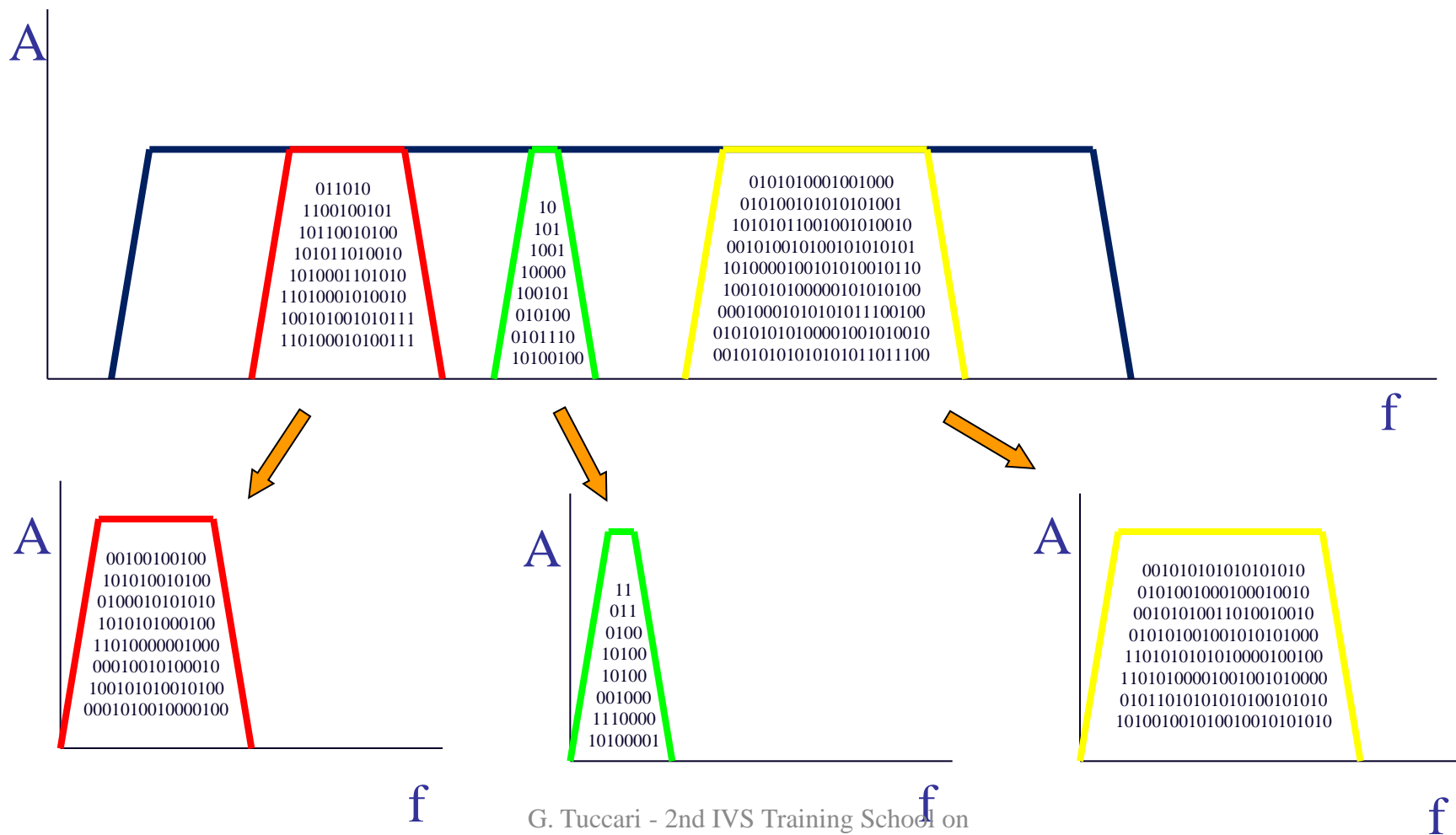


Frequency Conversion Chain



Different modes for converting

DDC - Digital Down Conversion to Base Band of Independent Channels



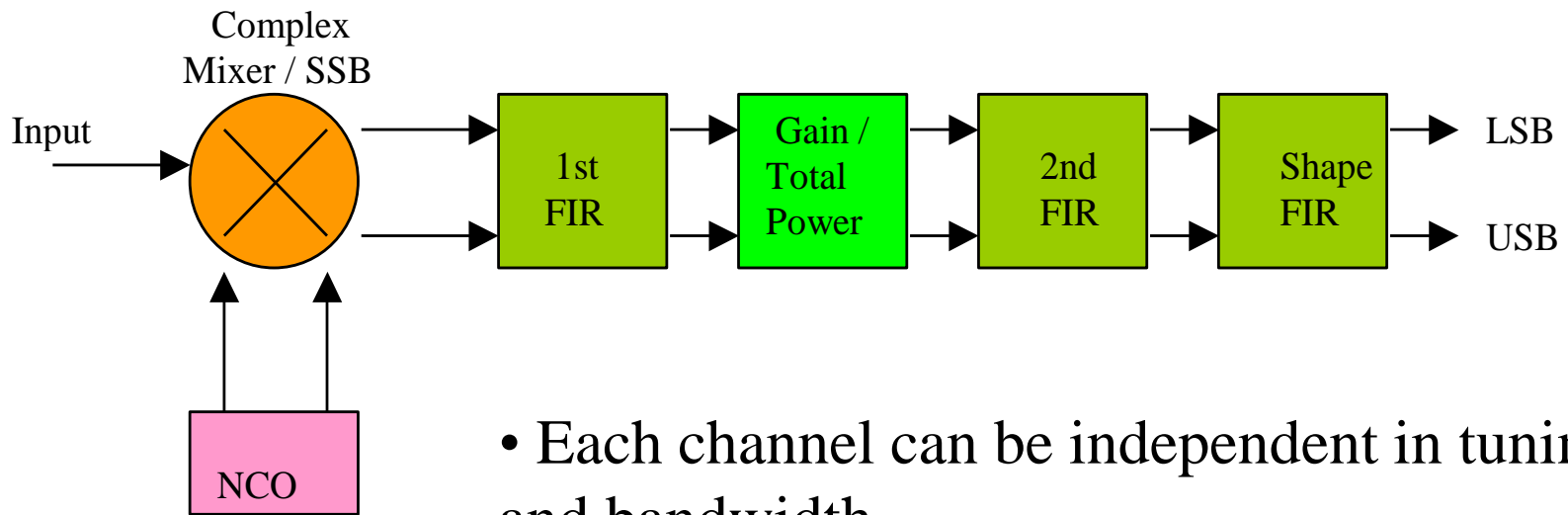
DDC - Digital Down Converter Configuration

- Direct conversion typically between high data rate sampled IF band and lower data rate base band
- LO as a Numerically Controlled Oscillator
- Mixer as Complex as Look Up Table multiplier
- Low-pass band filter Finite Impulse Response (FIR) filters cascade
- Decimation because of the high ratio between IF and output data rate performed with multirate/multistage FIR

Example of requirements in a Digital Down Converter

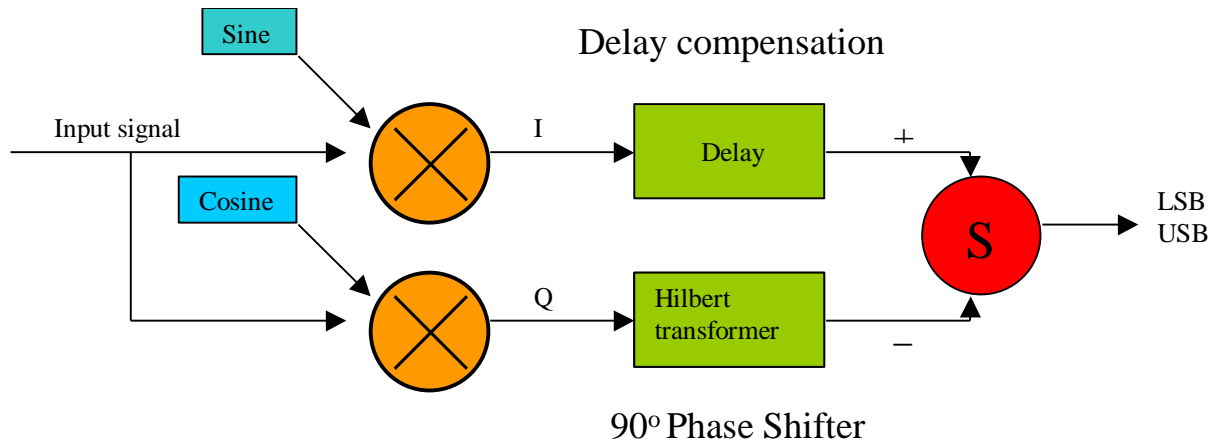
- Digital Total Power measurement at IF level
- Digital Total Power measurement at base-band level
- Gain Control
- Narrow bandwidth: 16, 8, 4, 2, 1, 0.5, 0.25 MHz
- Wide bandwidth: 512, 256, 128, 64, 32 MHz

DDC - Digital SSB Schematic View



- Each channel can be independent in tuning and bandwidth
- More channels possible

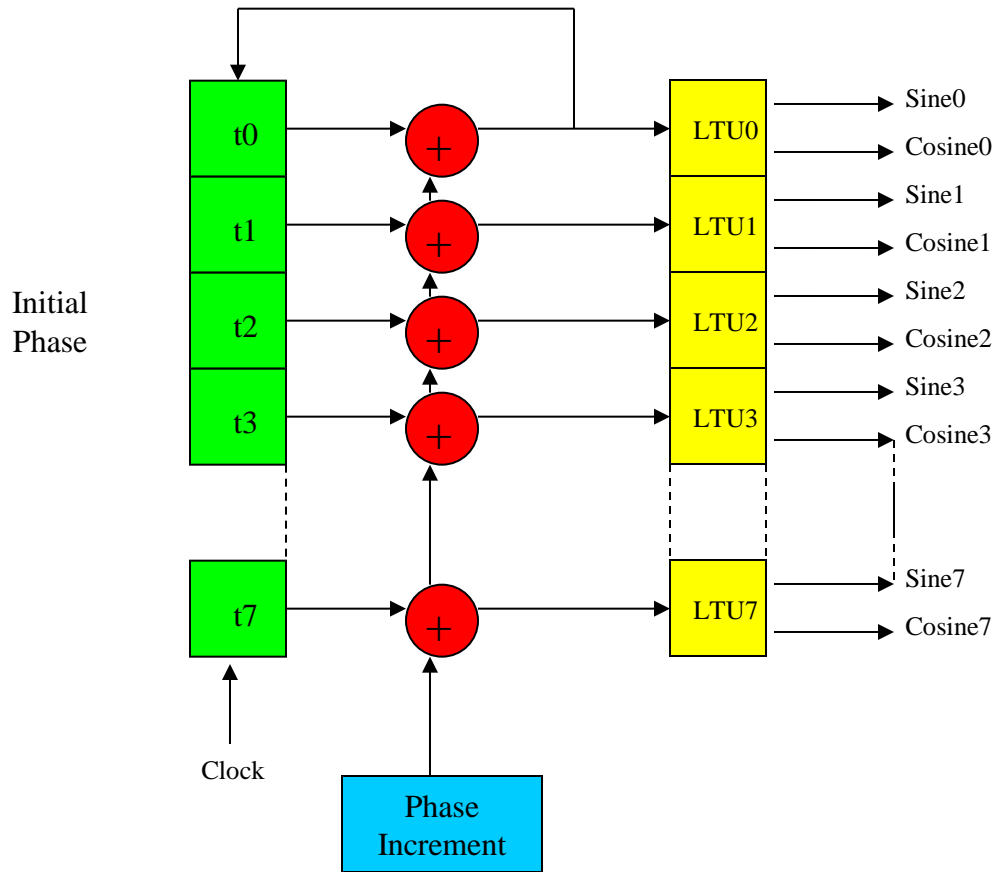
DDC - SSB Mixer Phasing Method



DDC - Example of SSB Down Converter Configuration Elements

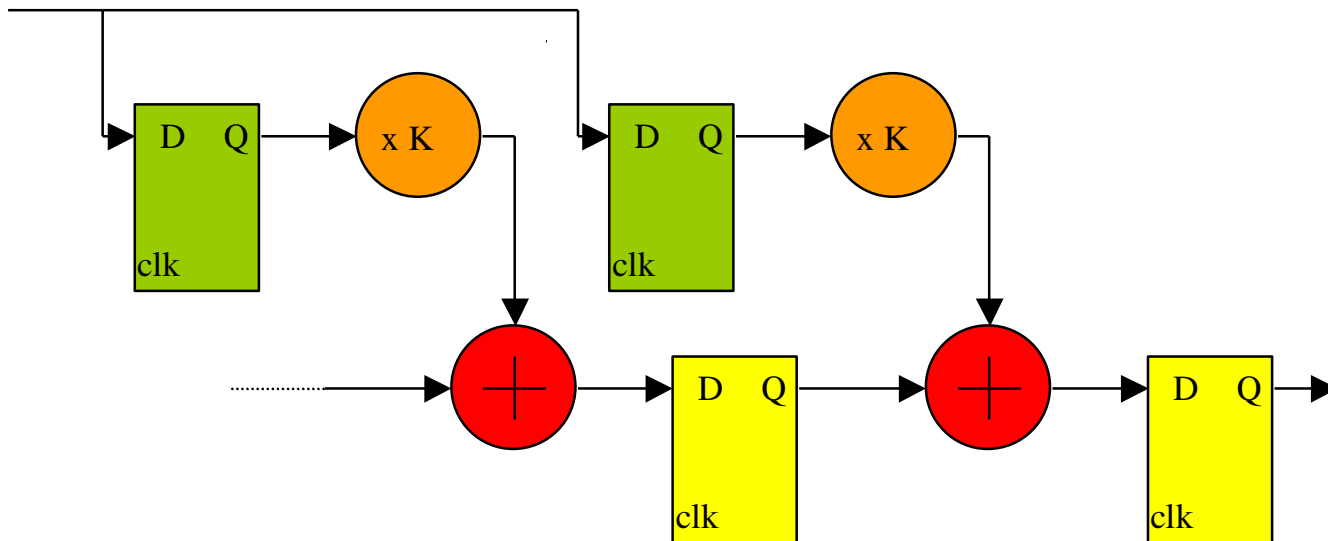
- Parallel data buses flow
- Output clock 32 MHz
- Parallel Pre-computed Oscillator
- Multistage FIR filtering
- Hilbert Transform filter
- Gain control
- Inverse distribute FIR typology
- Digital total power meter

DDC - Local Oscillator

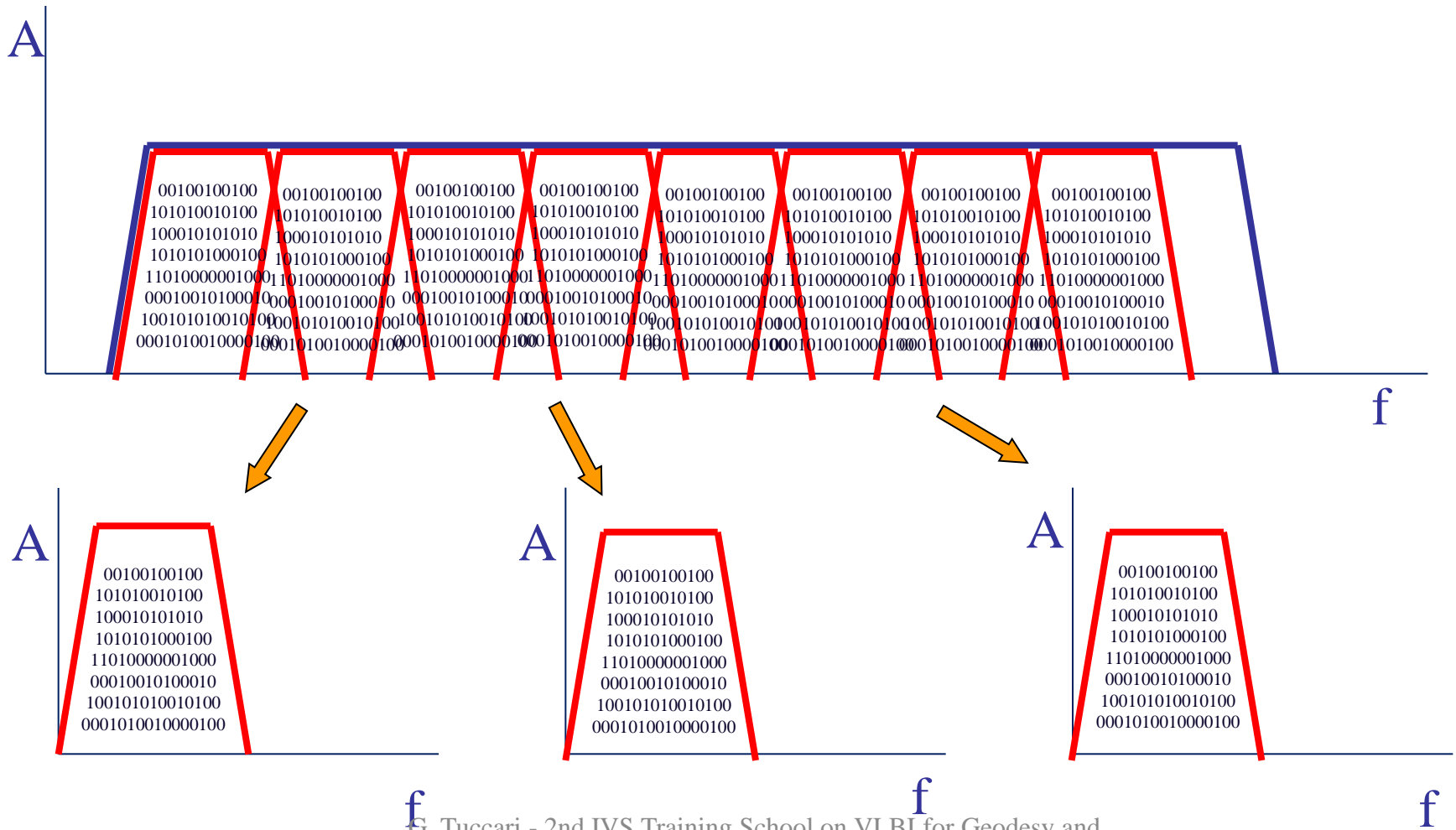


DDC - Inverse structure FIR (Finite Impulse Response) Filter

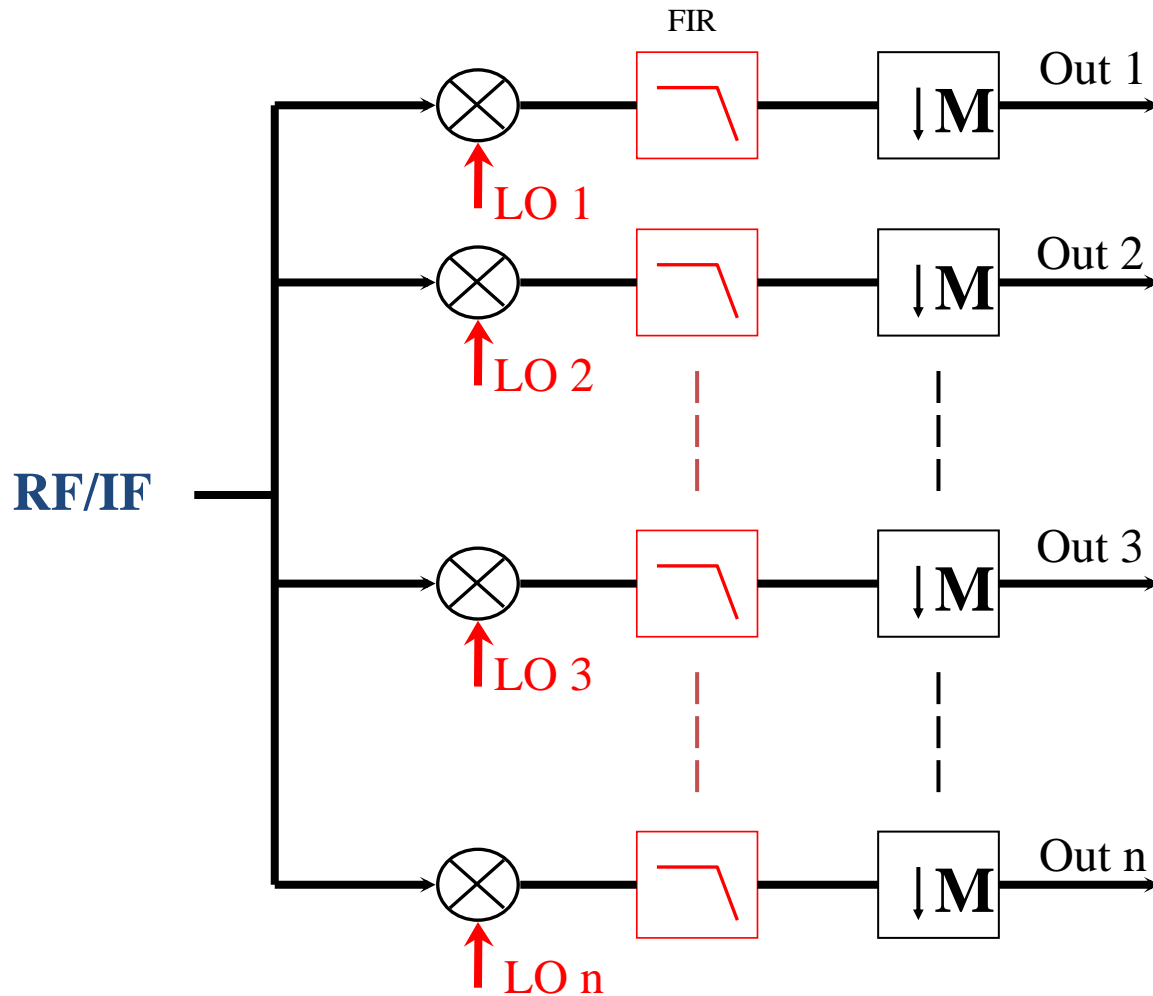
- Fully pipelined structure
- No multiple adders
- Distributed arithmetic
- Variable weights for dynamic shape control



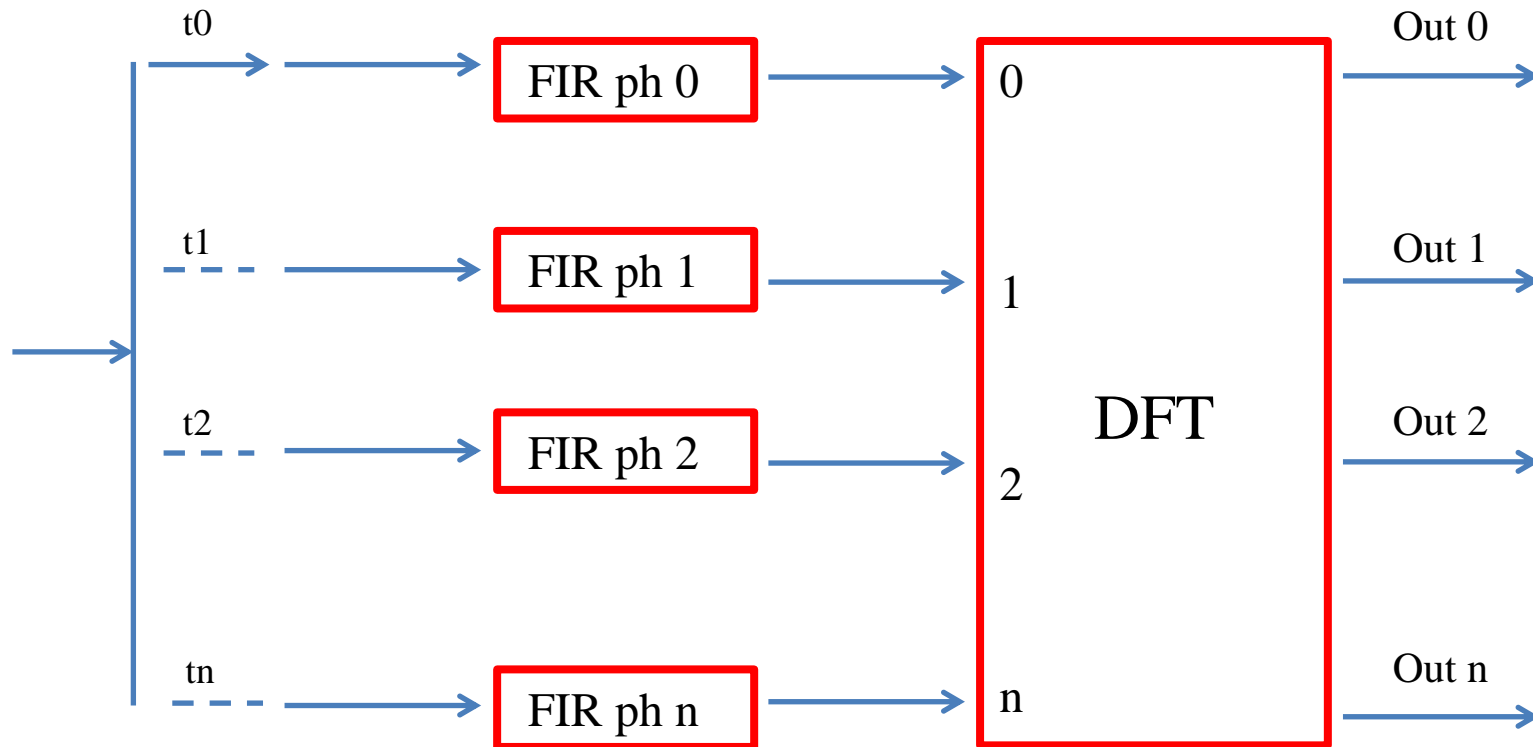
PFB - Multi Equispaced Channel Conversion to Base Band Polyphase Filter Bank



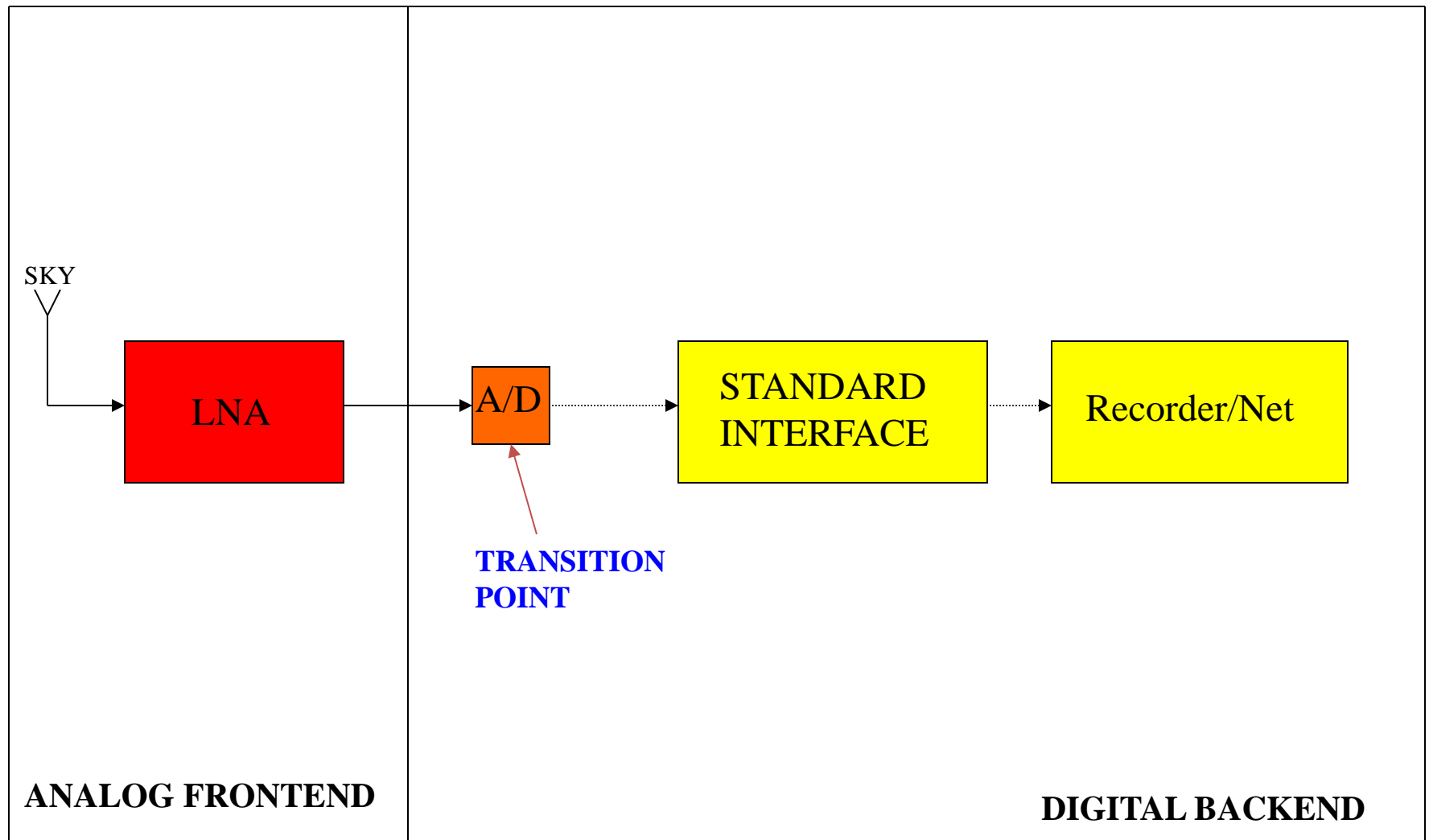
PFB - Multi Equispaced Channel Conversion to Base Band



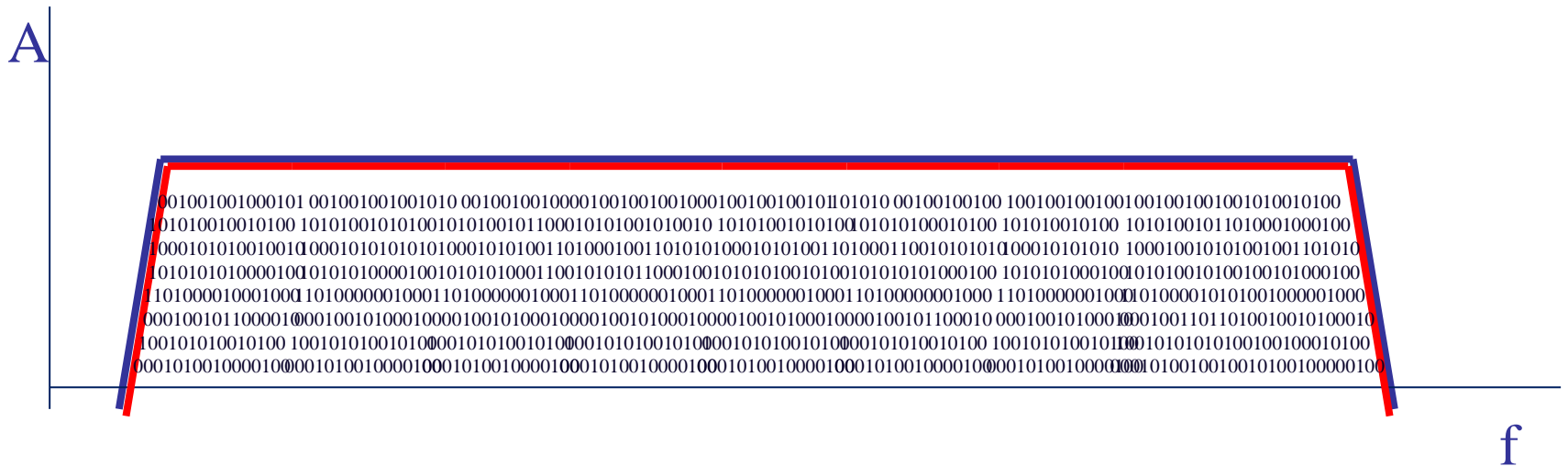
PFB – Poly Phase Filter Bank Solution



Future (and present) Front- and Backend Chain



DSC – Direct Sampling Conversion



DBBC Example

DBBC Back-ends evolution

DBBC1 2004 - 2008

in: 4 x IF-512MHz

out: **DDC** 16 x bbc (1-2-4-8-16MHz)@32MHz

0.512/1.024 Gbps

DBBC2 2007 – today

in: 4 x IF-512/1024MHz

out: **DDC** 16 x bbc (1-2-4-8-16-32MHz)@32/64MHz

PFB 4 x 16 x (32-64 MHz)@64/128MHz

4.096/8.192 Gbps

DBBC2010 2009 – today

in: 8 x IF – 512/1024MHz

out: **PFB** / **DSC**

16.384/32.768 Gbps

DBBC Back-ends evolution

DBBC3L (-2L2L) 2014 – today **EVN32Gbps / EHT**
in: 2 x IF-4096 / 4 x IF-2048 / 8 x IF-1024
out: **DDC** 8-16-32-64-128 MHz
PFB (and mixed) 32 - 64 -128 - 256 MHz
DSC 1024 - 2048 - 4096 MHz
16/32 Gbps

DBBC3L (-4L4H) 2014 – today **VGOS half-compliant**
in: 4 x IF-4096 / 8 x IF-2048 / 16 x IF-1024
out: **DDC** 8-16-32-64-128 MHz
PFB (and mixed) 32 - 64 -128 - 256 MHz
DSC 1024 - 2048 - 4096 MHz
16/32/64 Gbps

DBBC Back-ends evolution

DBBC3L (-8L8H) 2014 - today **VGOS full-compliant**
in: 8 x IF-4096 / 16 x IF-2048 / 32 x IF-1024 MHz
out: **DDC** 1-2-4-8-16-32-64-128-256 MHz
PFB PFB (and mixed) 32 - 64 -128 - 256 MHz
DSC 1024 - 2048 - 4096 MHz
16/32/64/128 Gbps

DBBC3H (-2H2H/-4H4H) end 2017 **VGOS full-compliant**
in: 2 x IF-14336 MHz
out: **DDC** 1-2-4-8-16-32-64-128-256-512-1024 MHz
PFB (and mixed) 32-64-128-256-512-256-512-1024 MHz
DSC 1024-2048-4096-8192-14336 MHz
16/32/64/128/229 Gbps

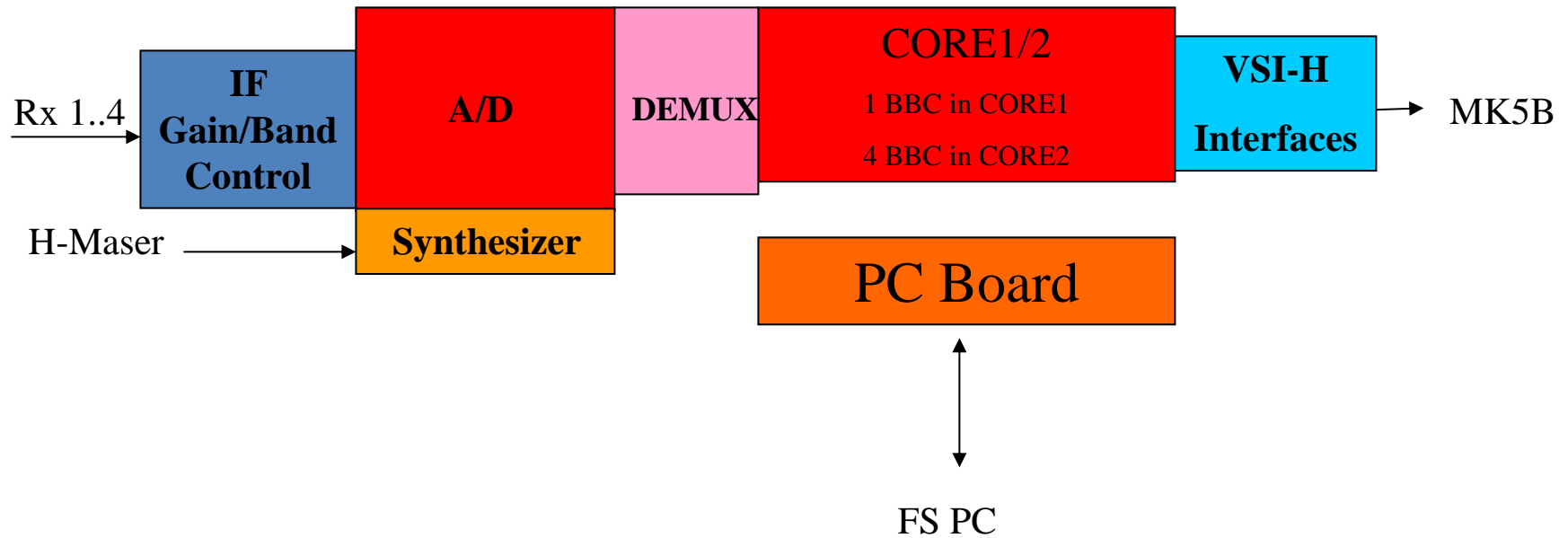
DBBC1 (2004) and DBBC2 (2007) General Features

- DBBC1: Four IF Input in the range 10-512 or 512-1024 MHz
- DBBC2: Four IF Input in the range 10-512, 512-1024, 1024-1536, 1536-2048, 2048-2560, 2560-3072, 0-1024 MHz, L band
- 1024 or 2048 (2000 for ALMA compatibility) MHz fixed frequency sampling clock
- DBBC1: Channel bandwidth ranging between 1MHz to 16 MHz
- DBBC2: Channel bandwidth ranging between 1MHz to 32 MHz
- Tuning step for VLBI 10 KHz
- Multiple architecture using fully re-configurable FPGA
- Modular realization for possible cascaded processing
- Field System support

DBBC1/2 General Features (cont.)

- Data out as single or double VSI interface
- Total power measurement capability
- Continuous Tsys measurement capability
- Digital to analog converter monitor output
- Digital AGC
- Optional 10 gigabit data shifter (see later)

DBBC1 General Schematic View



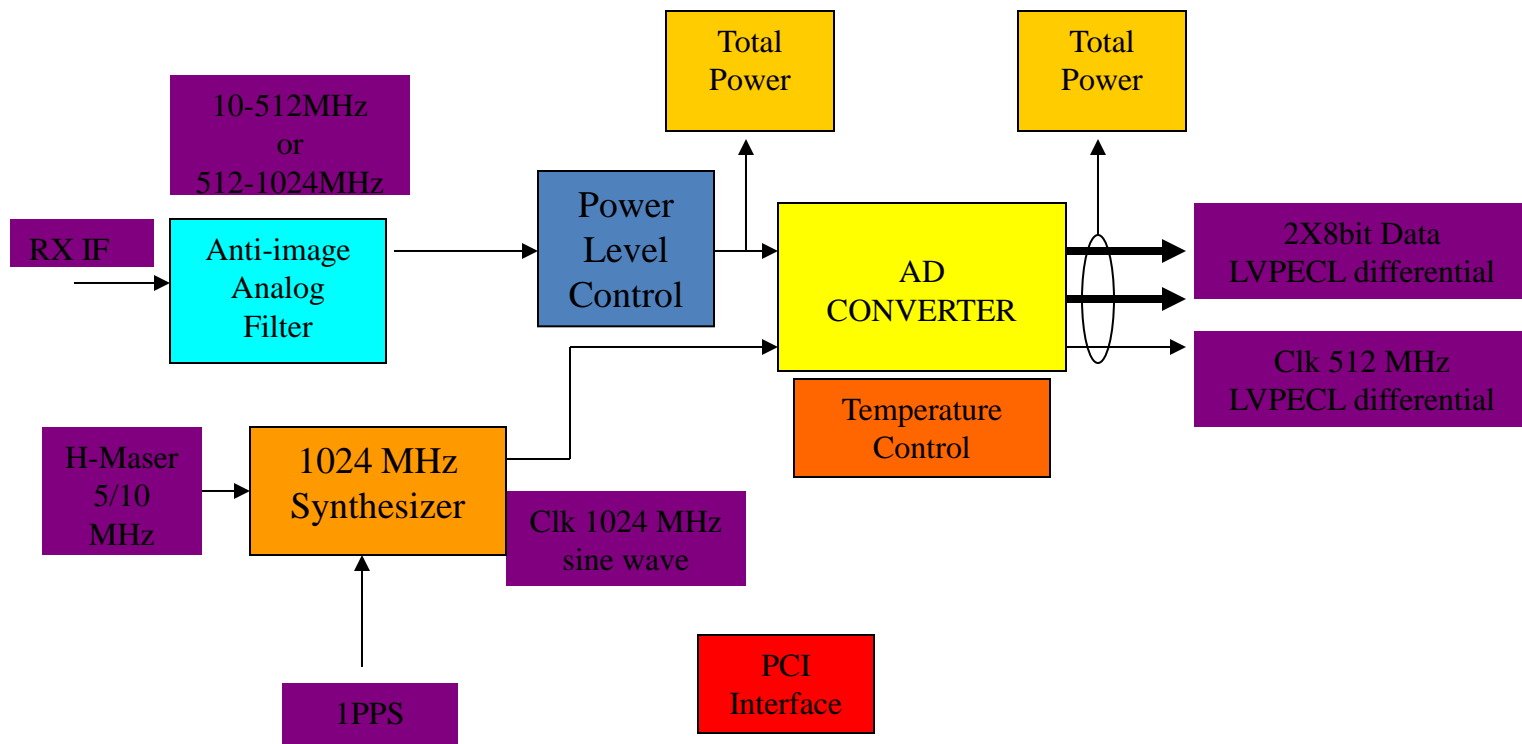
System Components

- Analog to digital converter 'environment': CoMo and ADB1/2
- 1024 MHz Synthesizer
- CORE1/2 Board
- FPGAs Core Configurations
- PCI interface
- VSI-H output
- Linux PC Board: System Management Software
- Optional Modules: 10 Gb/s output

Analog to digital converter board and Conditioning Module

- Conversion Clock 1024 MHz
- MAX108
- Front-end power level control
- Bandwidth 10-512 / 512-1024 MHz selection/filtering
- Pre- and post-conversion total power measurement
- AD temperature stabilization
- LVPECL level data bus
- PCI interface
- 1024 MHz Synthesizer

A/D Board Schematic View



DBBC Core1/2 Processing board

- A single module able to process more channels
- More modules can be cascaded
- Three external buses: HSI, HSO, HSC
- HSI Input data bus is propagated with very low skew
- HSO Output data bus is shared for multiple IF access
- HSC Control/Configuration bus

DBBC CORE1/2 Board Modes

- Different configuration can be supported:

(example)

SSB down converter

Wide band parallel FIR

Polyphase FIR / FFT

DBBC CORE1/2 Module Features (cont.)

- Different modules with different number of gates are supported for different functionalities
- Std. CORE module FPGA based
- DBBC1: A single board CORE1 can handle 1 independent narrow

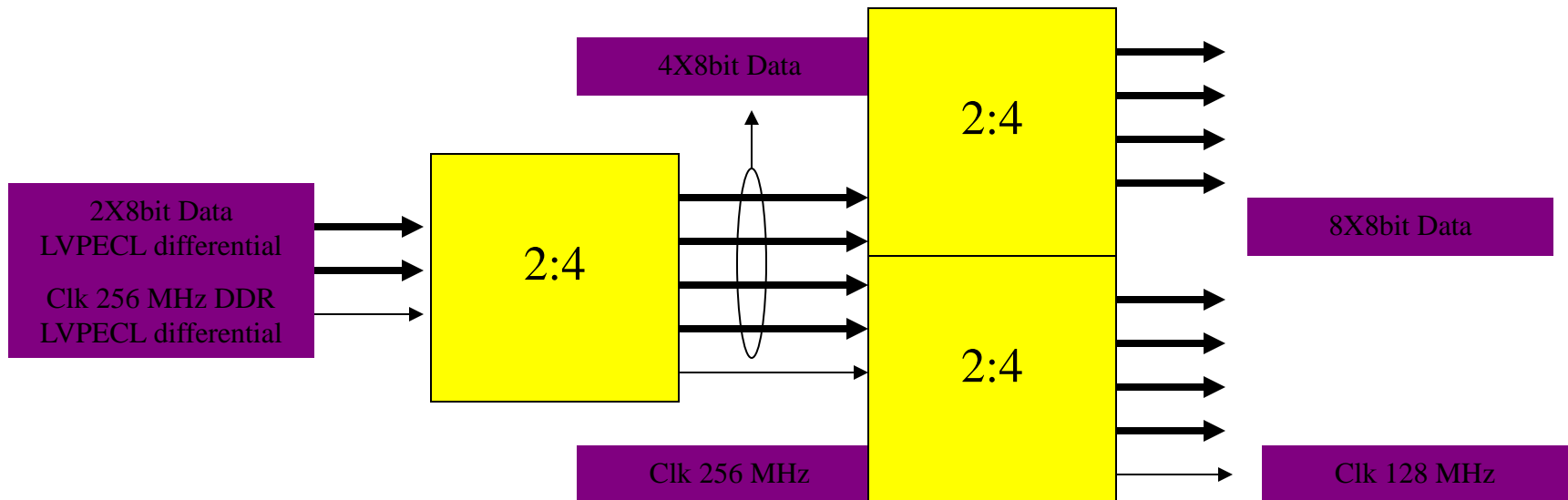
band LSB&USB channels

- DBBC2: A single board CORE2 can handle 4 independent narrow band LSB&USB channels

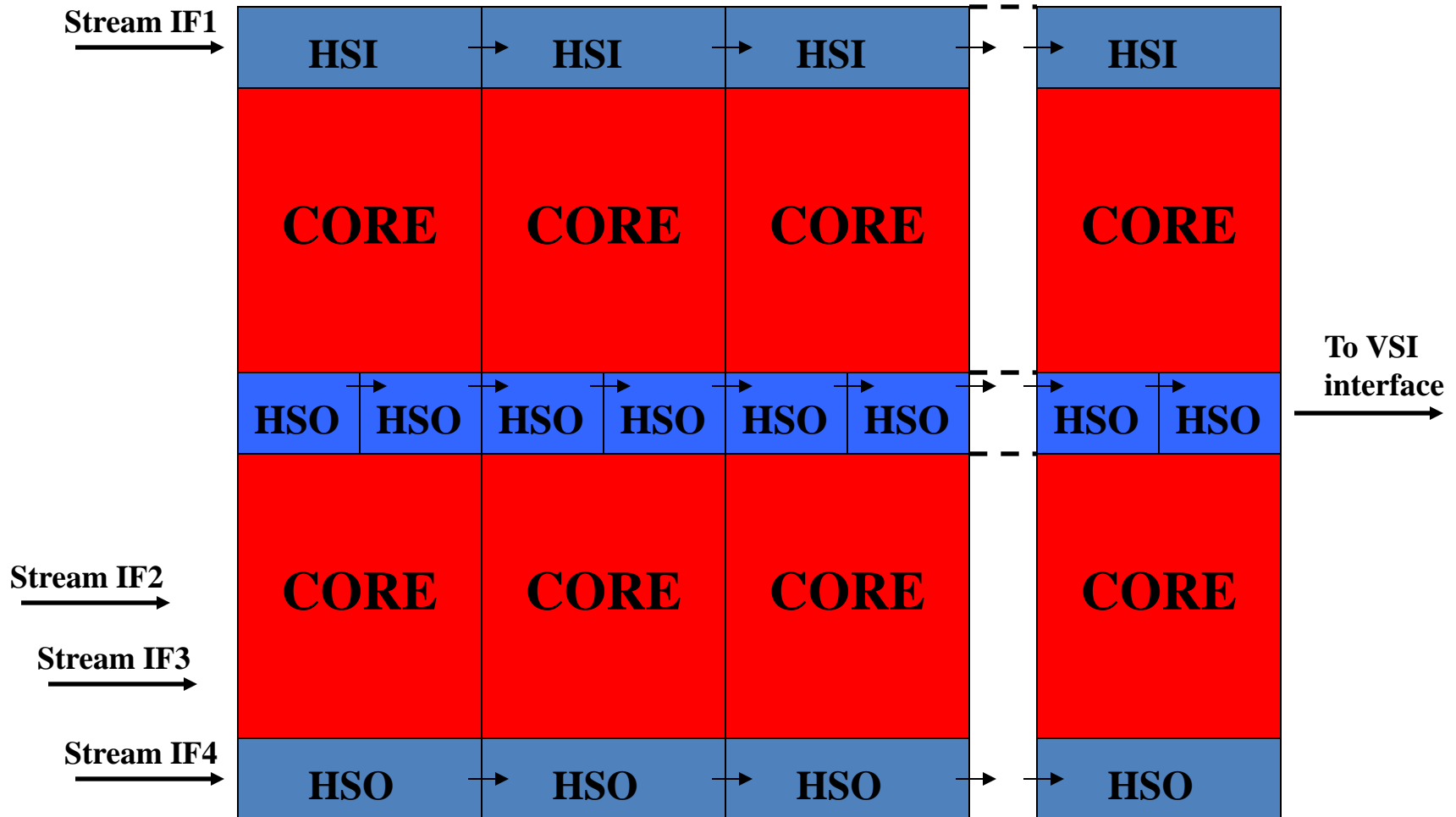
CORE1/2 Board

- HSI Cascadable Input Bus 8x8bit @128MHz
- HSO Shared Output bus 2x32bit @32,64MHz
- HSC Control / Configuration bus 32bit
- HSX Internal data bus 128bit @max128MHz
- Maximum 4 FPGA VirII-1152pin
- 1 FPGA VirIIPro for low level computation
- PCI interface
- ‘Sandwich’ cascade method

COR1/2 includes 2:8 Demultiplexer

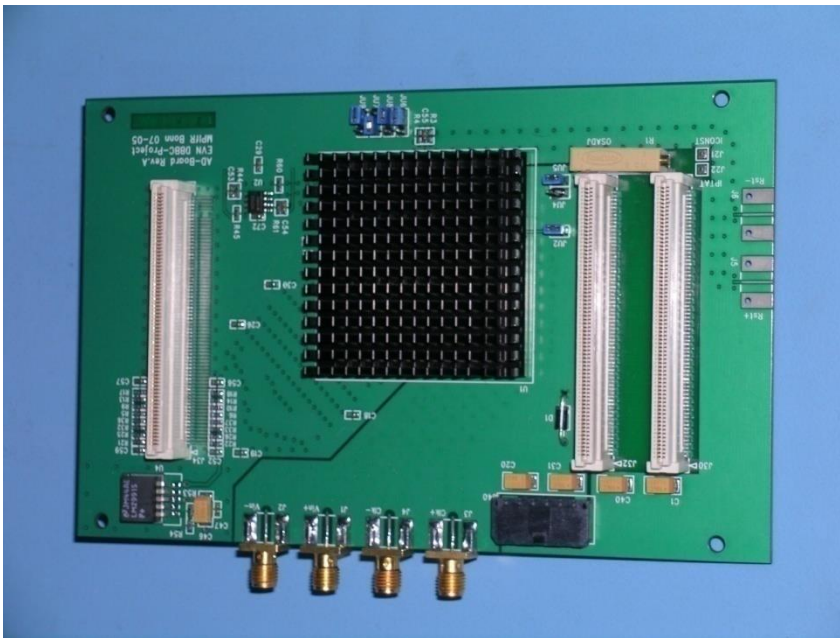


CORE1/2 Modules Cascade Architecture



ADB1

Analog to Digital Converter



Analog input: 0 - 2.2 GHz

**Max Sampling clock single board:
1.5 GHz**

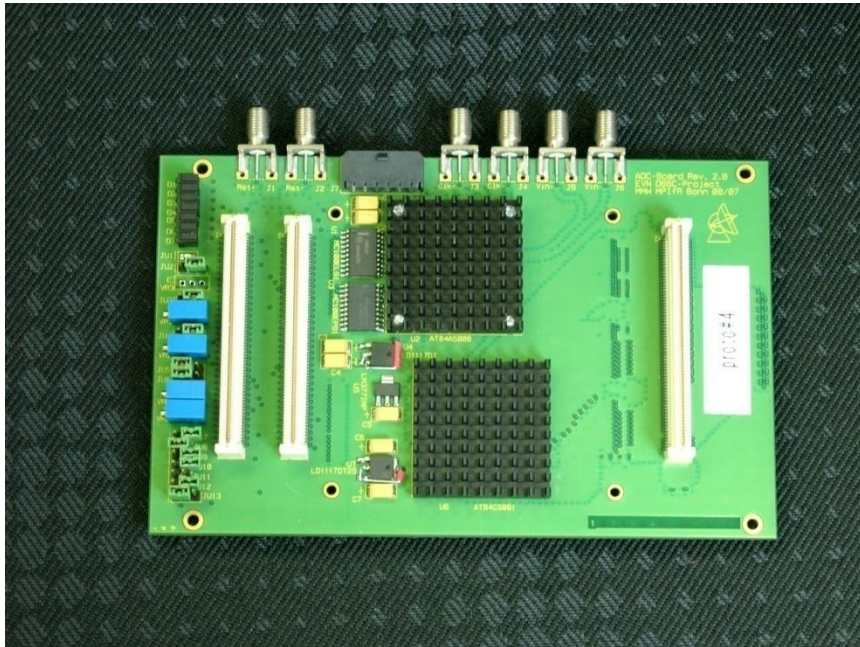
**Max Instantaneous Bandwidth in Real
Mode: 750 MHz**

**Max Instantaneous Bandwidth in
Complex Mode: 1.5 GHz**

Output Data: 2 x 8-bit @ $\frac{1}{4}$ SClk DDR

ADB2

Analog to Digital Converter



Analog input: 0 – 3.5 GHz

**Max Sampling clock single board:
2.2 GHz**

**Max Instantaneous Bandwidth in Real
Mode: 1.1 GHz**

**Max Instantaneous Bandwidth in
Complex Mode: 2.2 GHz**

**Output Data: 2 x 8-bit @ 1/4 SClk DDR
4 x 8-bit @ 1/8 SClk DDR**

**Piggy-back module support for 10-bit output
and connection with FiLa10G board.**

CORE2

Basic processing unit



Input Rate:

(4 IFs x 2 bus x 8 bit x SClk/4 DDR) b/s

(2 IFs x 4 bus x 8 bit x SClk/8 DDR) b/s

More...

Typical Output Rate:

(64 ch x 32-64-128-256) Mb/s

Programmable architecture

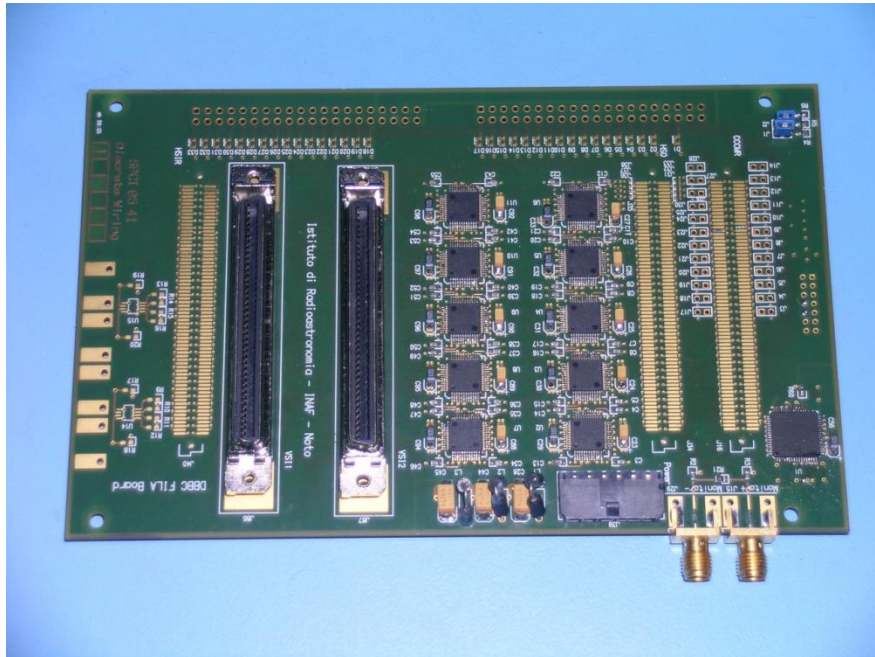
Es. Digital Down Converter:

1 CoreBoard2 = 4 BBC

Max Input/Output Data Rate 32.768 Gbps

FiLa

Connection and Service



First and Last board in the stack

First:

**Communication Interface
JTAG Programming Channel
1PPS Input**

Last:

**2 VSI Interfaces
DA Converter
1PPS Monitor Out
80Hz Continuous Cal Out**

CaT

Clock and Timing

Timing Board



**Timing Synchronization:
High Resolution UT1PPS Generation**

Clock Board



**System Clock Generation:
Input Reference
Programmable
(es. 1024 MHz, 2^{30} Hz,
2048 MHz, 2^{31} Hz)**

ConditioningModule



Pre-AD Conversion Analog Signal Conditioning

Pre-AD Conversion Band Definition

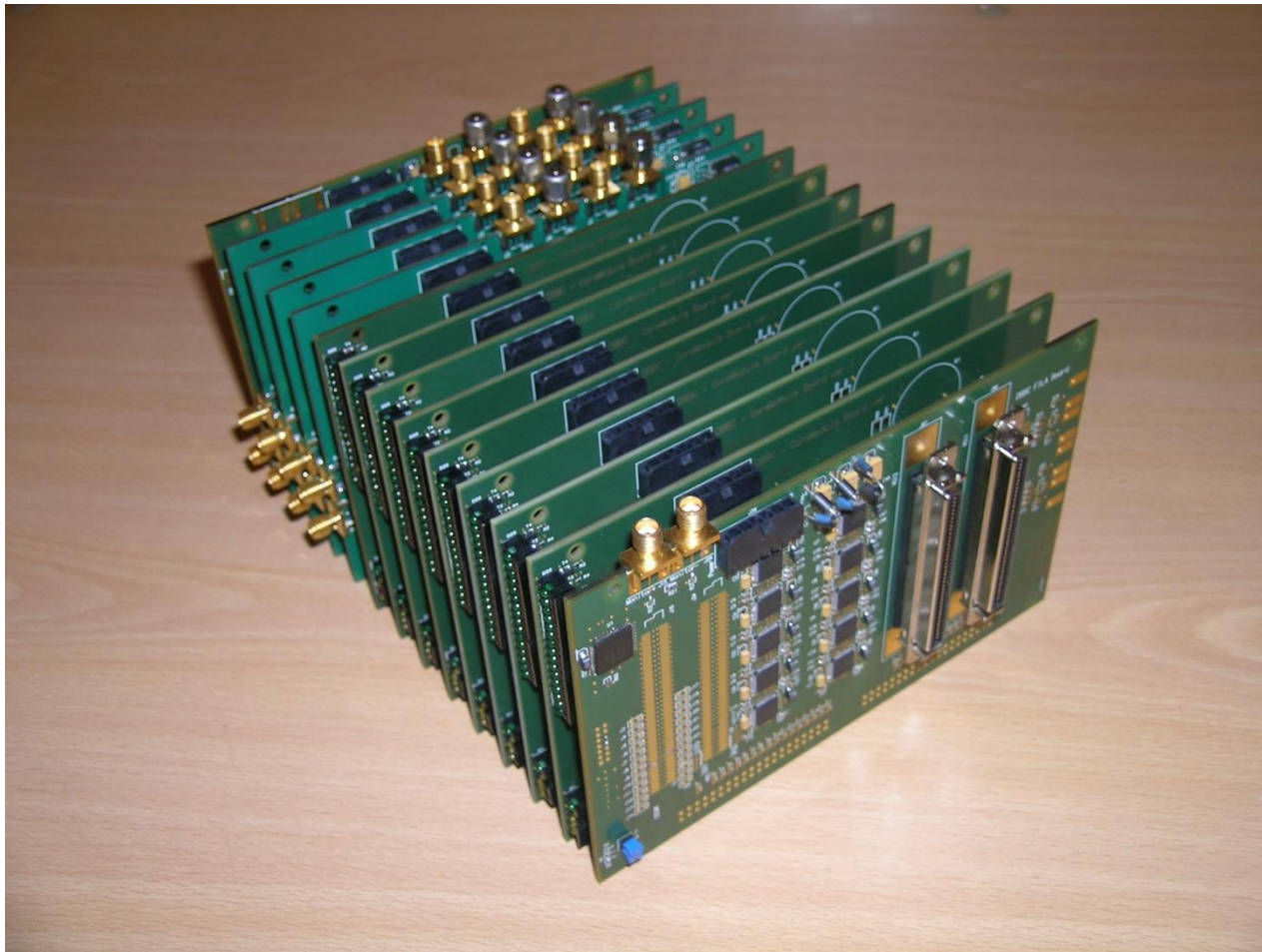
4 IFs Selectable Input

Total power measurement

RF Gain Control

Amplitude equalization

4 ADB1 + 8 CORE1 Stack



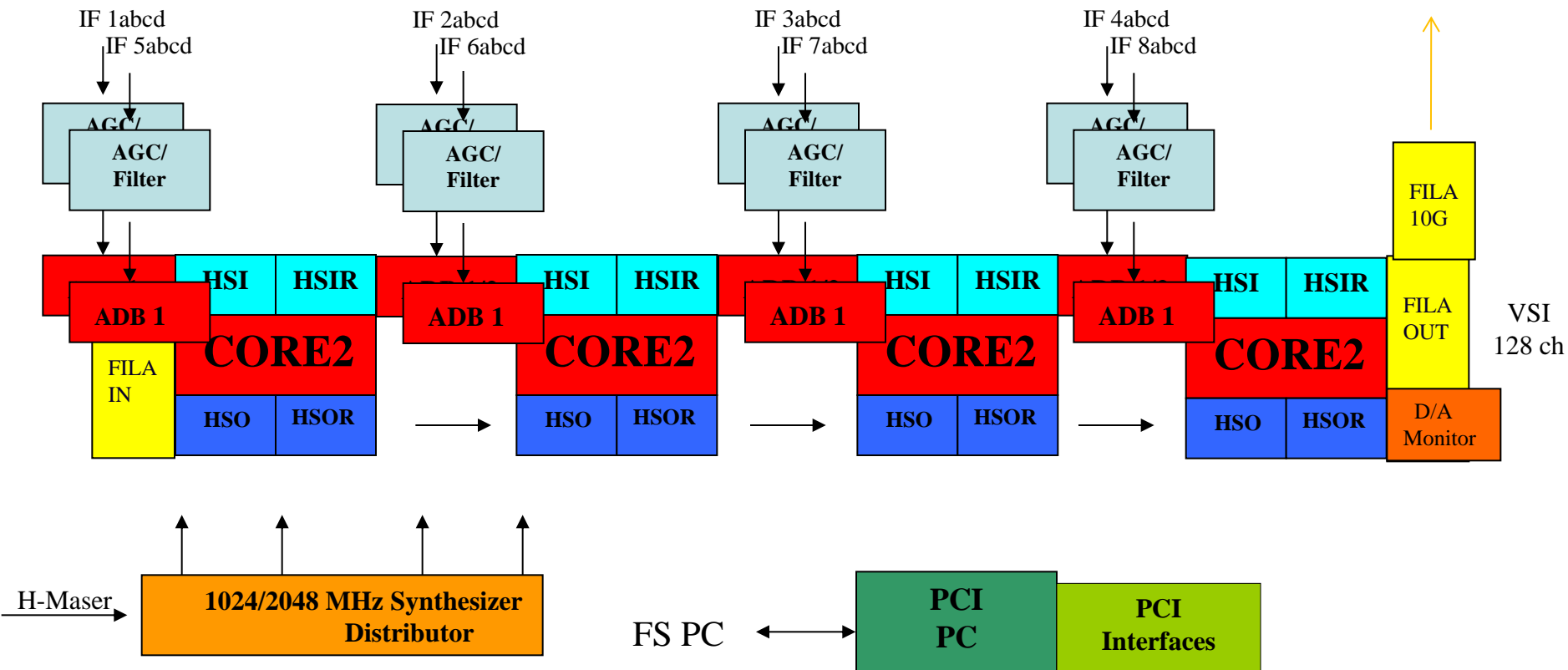
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DBBC2010 Architecture A

8 IFs @ 512 MHz

Output data rate 16Gbps

IF_n (MHz)
 1~512, 512~1024, 1024~1536, 1536~2048

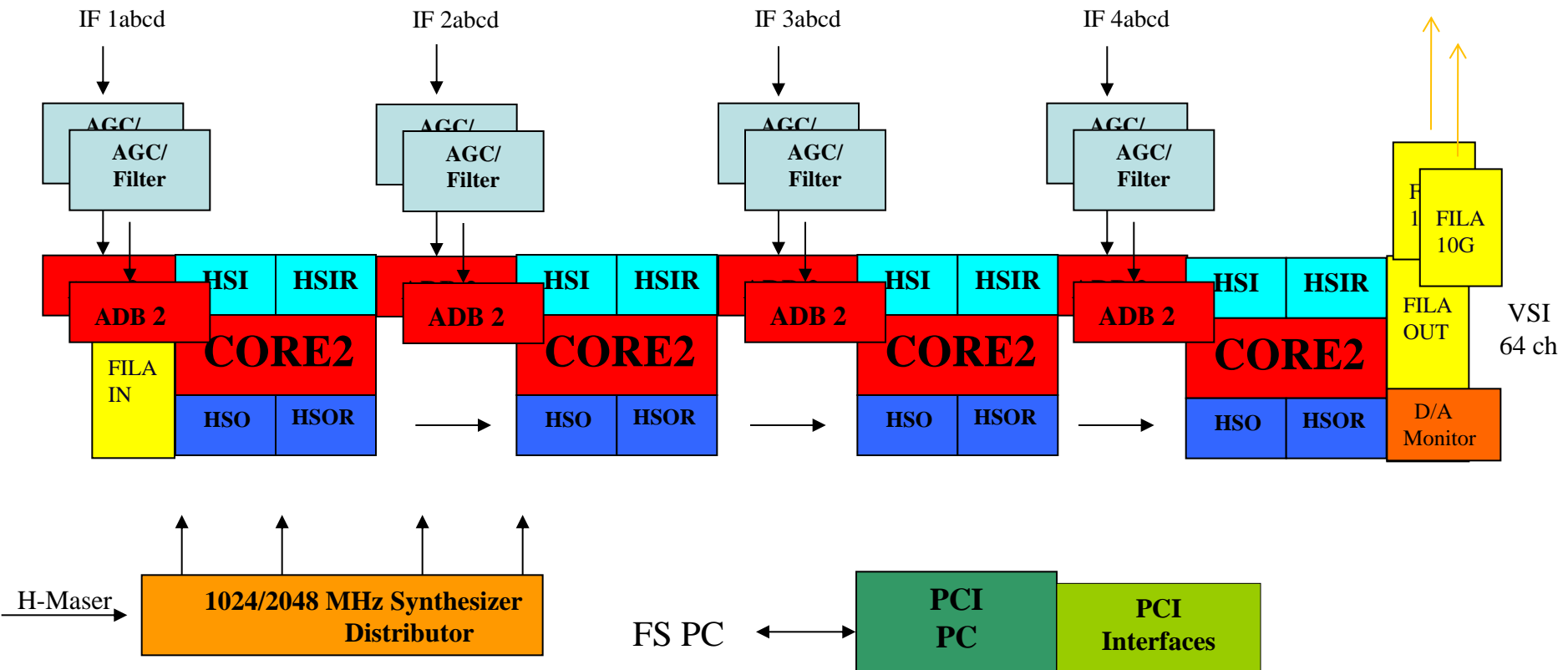


DBBC2010 Architecture B

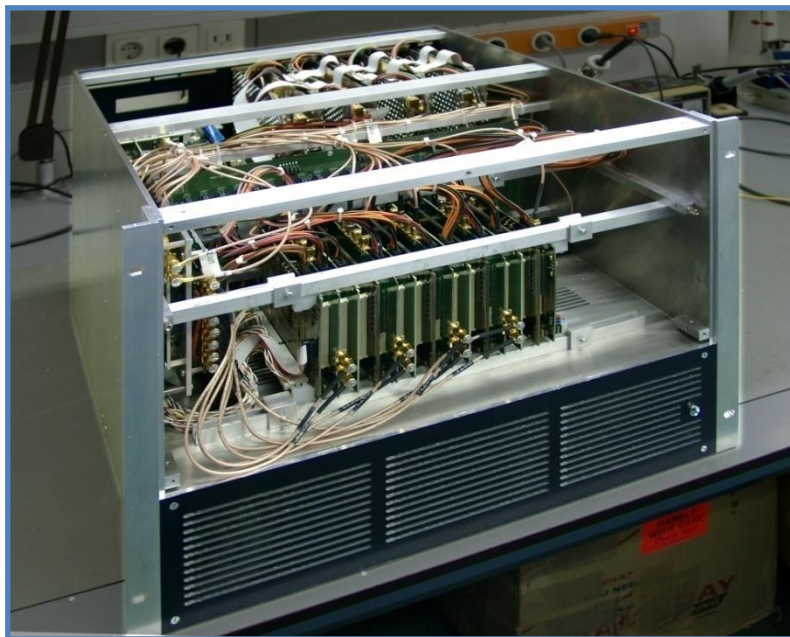
8 IFs @ 1024 MHz

Output data rate 32Gbps

IFn (MHz)
0~1024, 1024~2048, 2048~3072 MHz



DBBC1/2 photos



Network Board

FILA10G

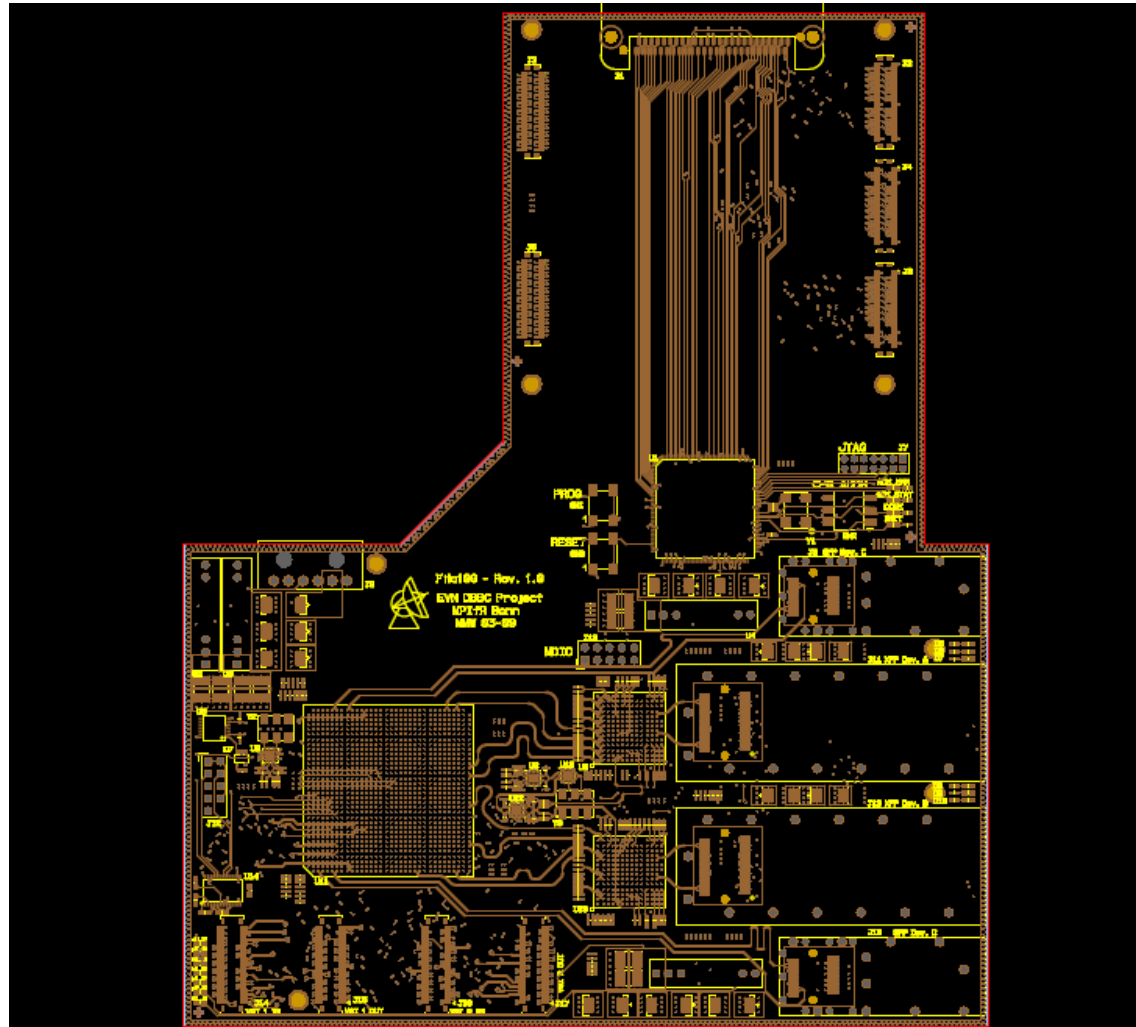
- FILA10G the interface between the DBBC (or any VSI device) to 10G network
- The board shifts interface for the MK5C or as direct connection to the network at 1–2–4–10–20 Gbps
- Can be used as standalone between VSI and network
- Can be used as standalone with ADB2
- MK5B and VDIF compliant (corner turner included)

10GE Output Stream

Output is a set of 10GE connections (optical or copper):

- MK5B
- VDIF - Multichannel single thread
- VDIF - Corner turned data with multiple threads carrying single band channels
- Multiple destination address for the multiple threads in the data streams
- Raw

FiLa10G



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FILA10G

Shifts VLBI data on Internet – 16 Gbps 4 x VSI-H <> 2 x 10GE

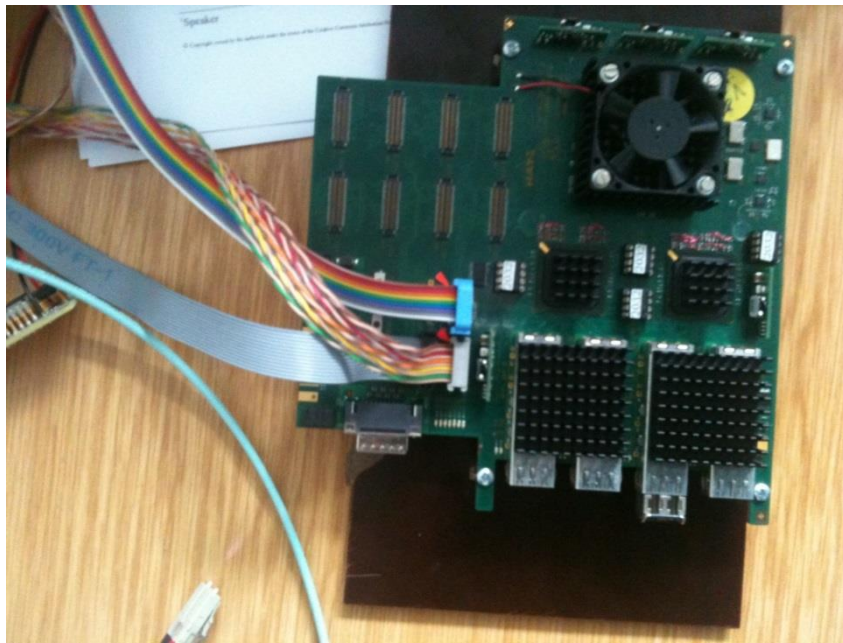
- MK5B up to 4 Gbps
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads
- RAW (no headers)
- Threads eventually corner-turned
- The 10G Ethernet ports independent in destination address in VDIF-ST and MK5B
- Multi-thread mode support an independent block of destination addresses
- Decimation and bit-mask selectable



FILA10G-S4

- MK5B up to 4 Gbps
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads
- RAW (no headers)
- Threads eventually corner-turned
- The 10G Ethernet ports independent in destination address in VDIF-ST and MK5B
- Multi-thread mode support an independent block of destination addresses
- Decimation and bit-mask selectable

**Shifts VLBI data on Internet – 32 Gbps
8 x VSI-H \leftrightarrow 4 x 10GE**



DBBC3 (2014)

- Development started for a new set of boards to increase maximum bandwidth and data rate
- Compatible with precedent versions (replacement of boards in the stack, or mixed operation)
- New CoMo: 6 GHz bwd
- New CaT: integrates Clock and Timing boards and allow interleaved operations
- New Core3

DBBC3L (2014) Radionet 3

General Performance

- Number of RF/IF in one system: **std. 2 (8 for VGOS)**
- Instantaneous bandwidth each sampler: **4 GHz**
- Sampling representation: **10 bit**
- Processing capability: **std. 24 (max 96) TMACS** (multiplication-accumulation/s)
- Output: **VDIF 10GE/40GE packets, 32/64/128 Gbps**
- Observing Modes: **DDC/PFB/DSC**
- Compatibility with existing DBBC2 environment

DBBC3L is aiming at:

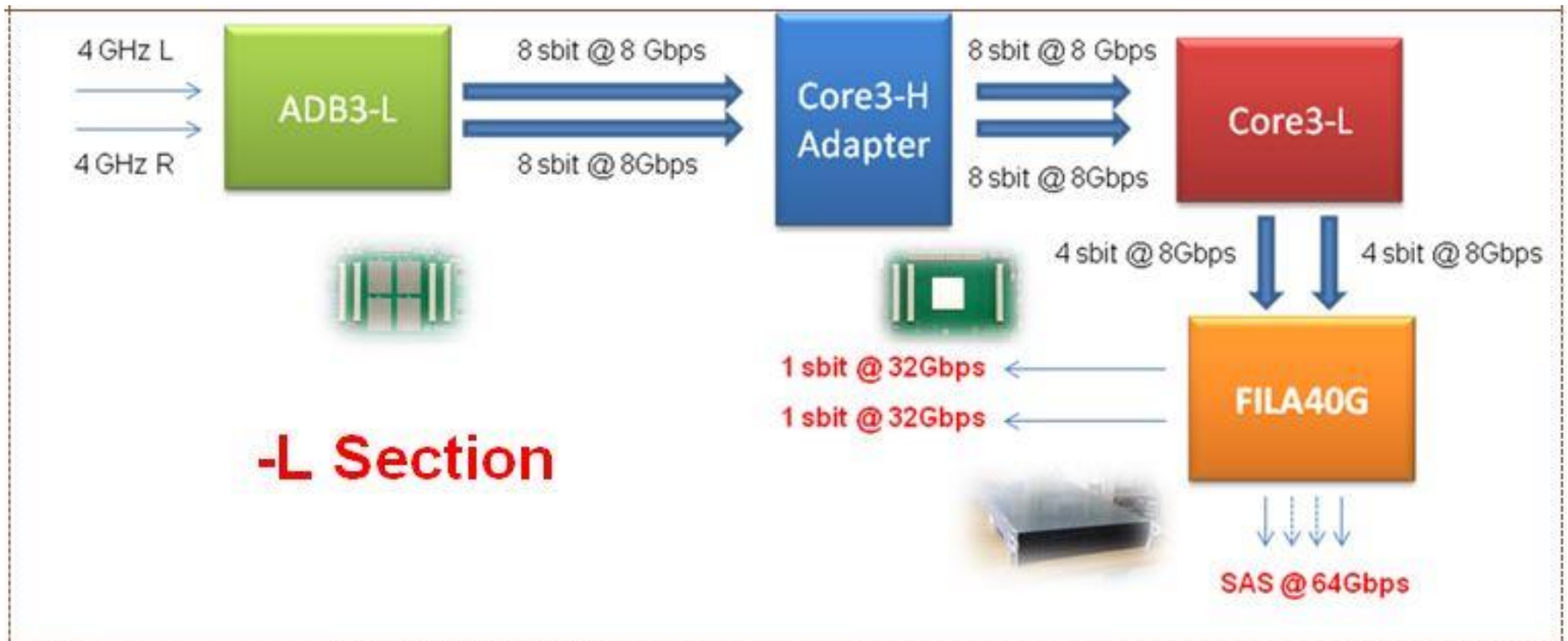
Astronomy

- **EVN wide-band VLBI backend**
- **EHT (Event Horizon Telescope)**

Geodesy

- **VGOS ultra-wide-band VLBI system**

DBBC3-L Architecture for EVN and EHT



GCoMo (GigaConditioningModule)

Additional element to adapt the receivers

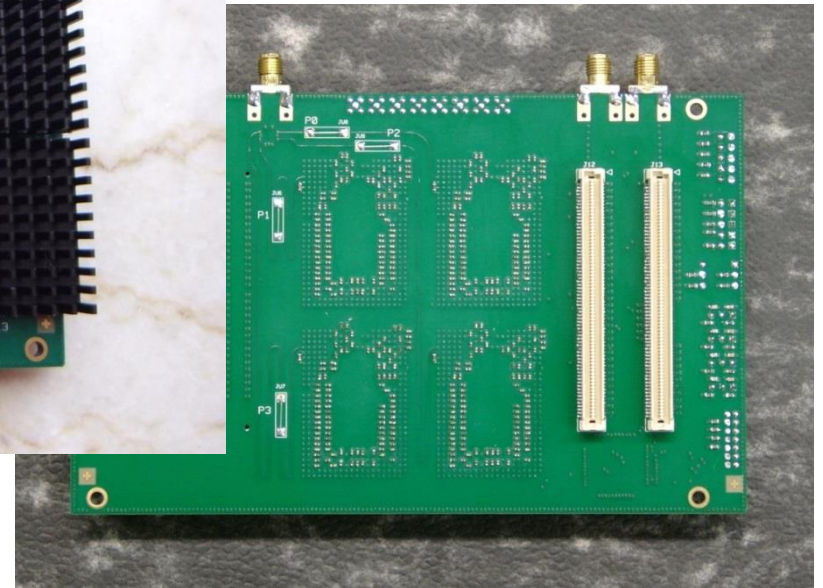
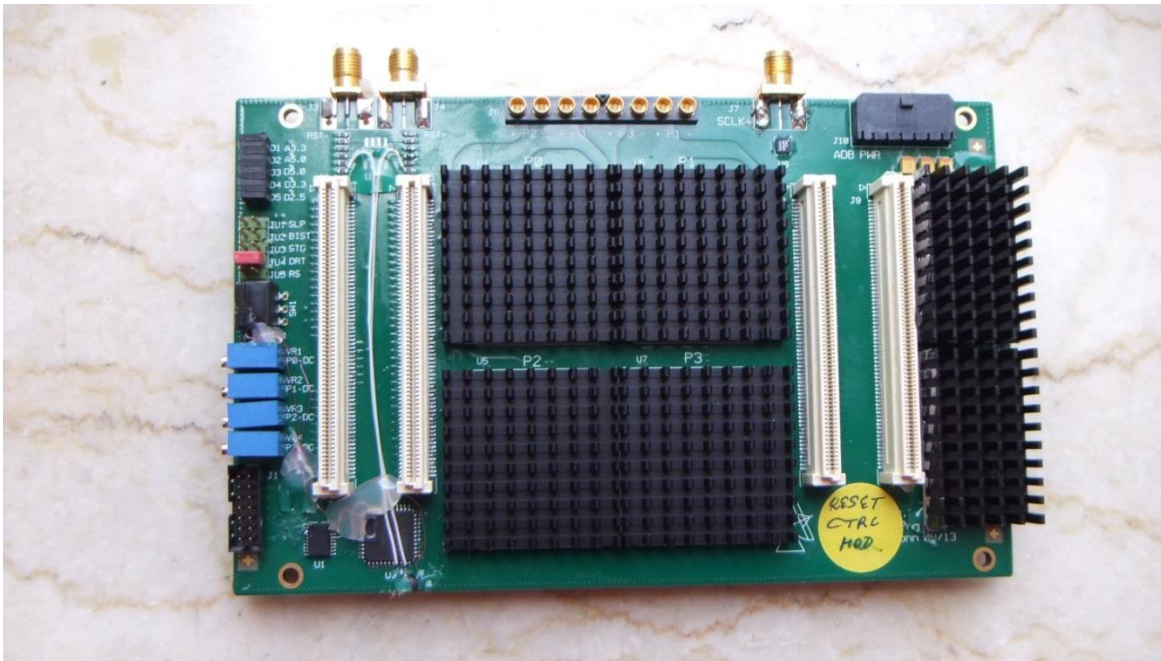
- Downconvert pre-filtered pieces of 4 GHz bandwidth
- Input range: up to 16 GHz
- Number of channels: 2 pre-filtered 4 GHz bands
- Total power detectors: 2 independent
- Power level control in agc and manual mode
- Compatibility with existing DBBC environment

ADB3L - Sampler board

- 4 x 1 GHz samplers combined
- Number of IFs: **1 - 4**
- Equivalent Sample Rate: **2-4-8 GSps**
- Instantaneous bandwidth: **1-2-4 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC environment

Status ADB3L

Prototype ready debugged, final revision under construction

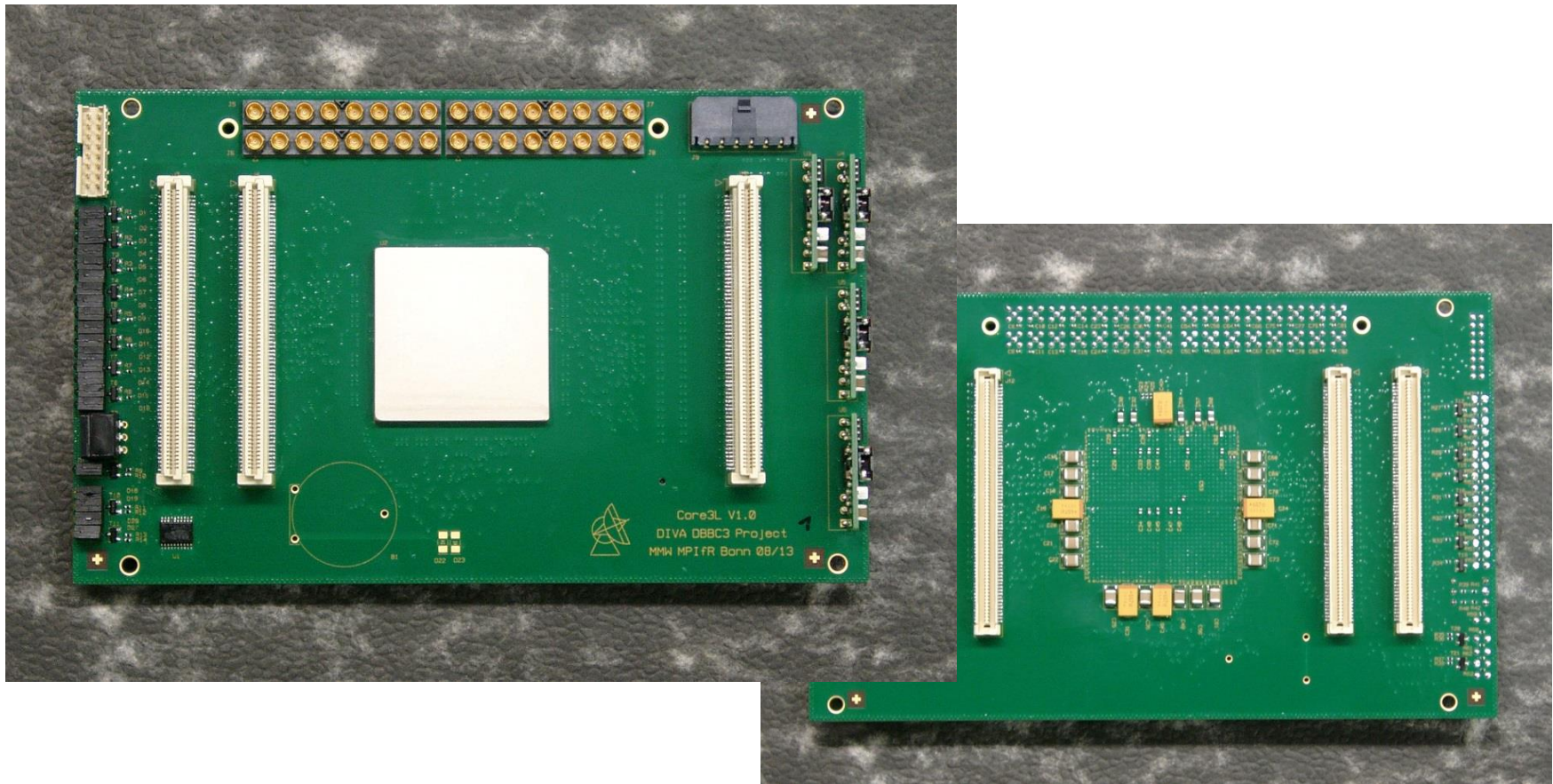


CORE3L - Processing board

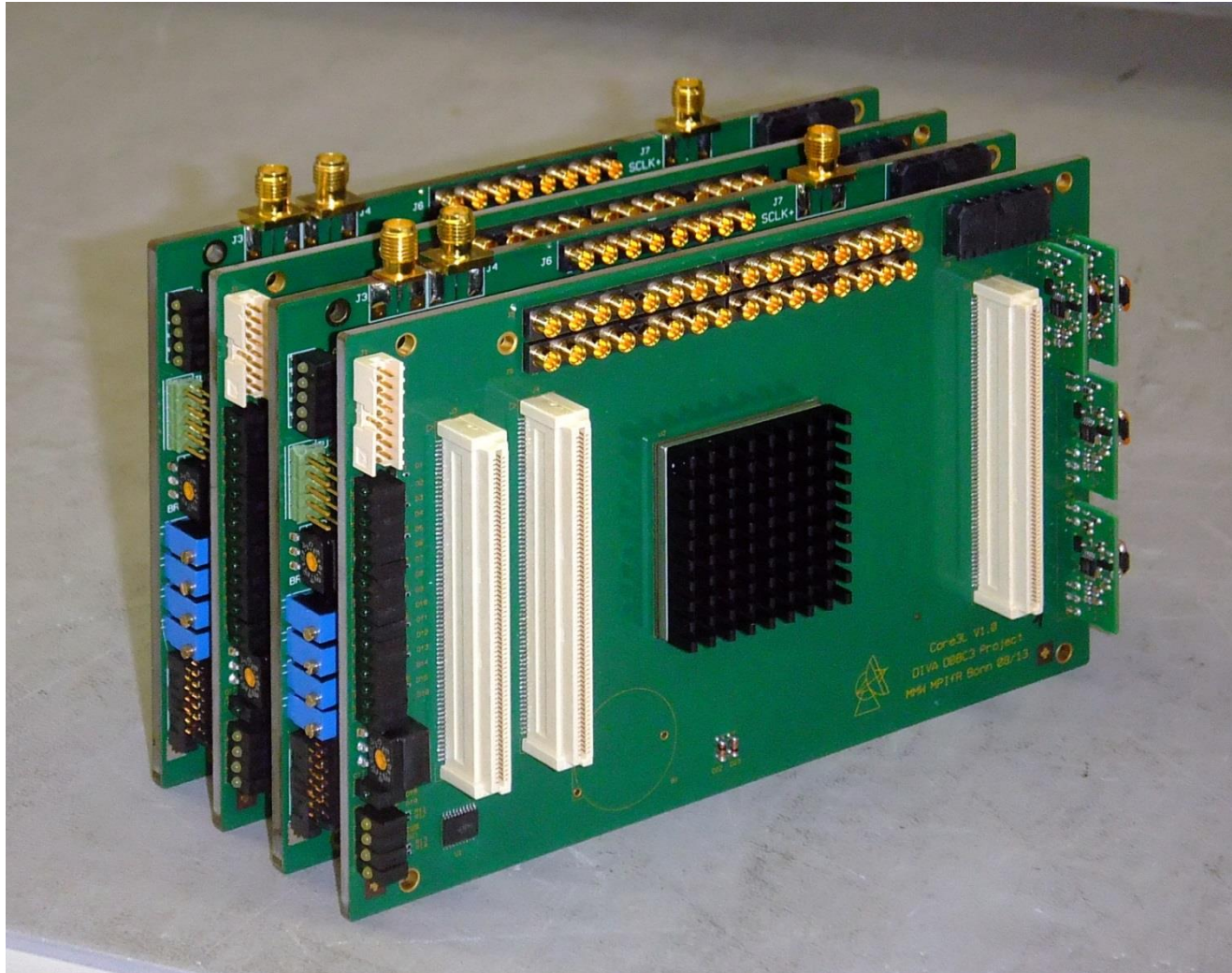
- Powerful FPGA (Field Programmable Gate Array)
- Number of I/O: **max 40 serial links 12.5Gbps**
- Number of Output: **max 32 serial links 11.2Gbps**
- Input Sampling Representation: **8-10 bit**
- Processing capability: **max 3 TMACS** (multiplication-accumulation per second)
- Processing capability: **DDC, PFB, WB-DDC, WB-PFB, DCS**
- Output: **VDIF 10GE packets**
- Compatibility with existing DBBC environment

Status CORE3L

Prototype debugged, final version under construction

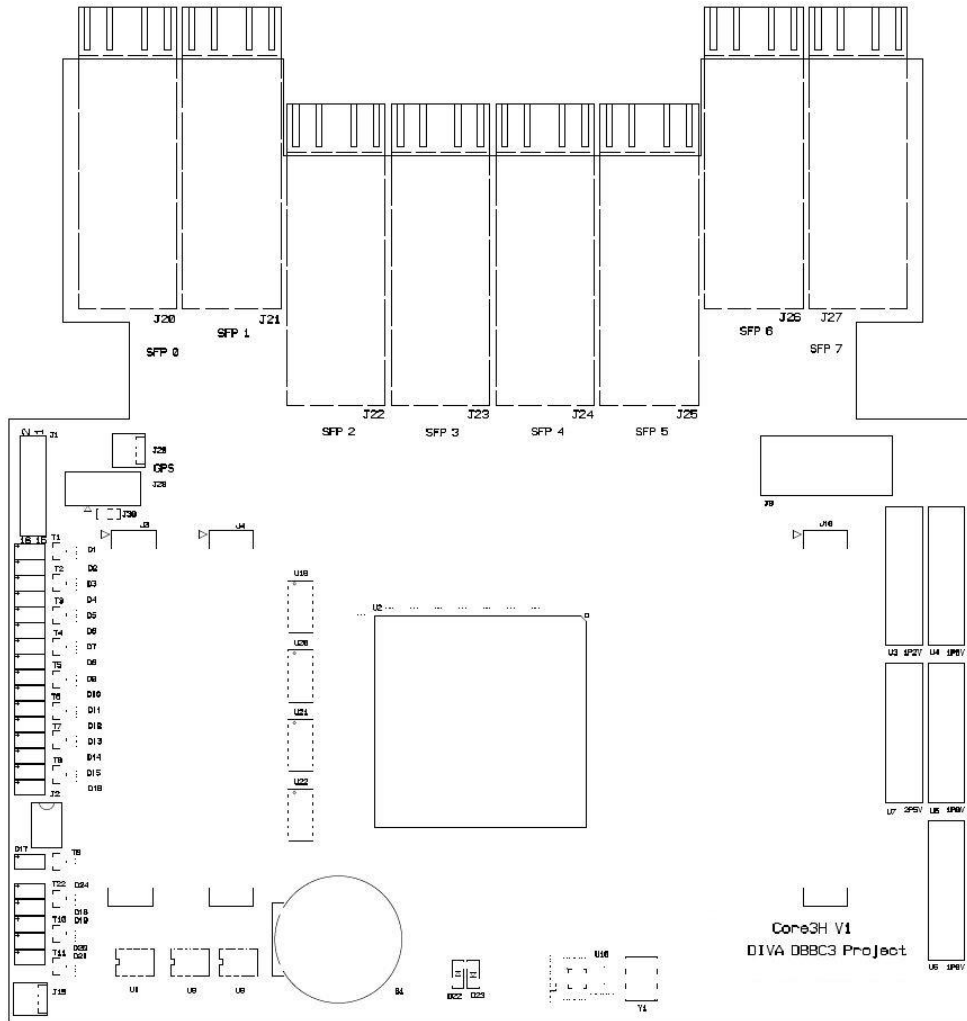


EVN/EHT: Stack with 2 ADB3L and 2 CORE3L 4 GHz bwd real dual polarization



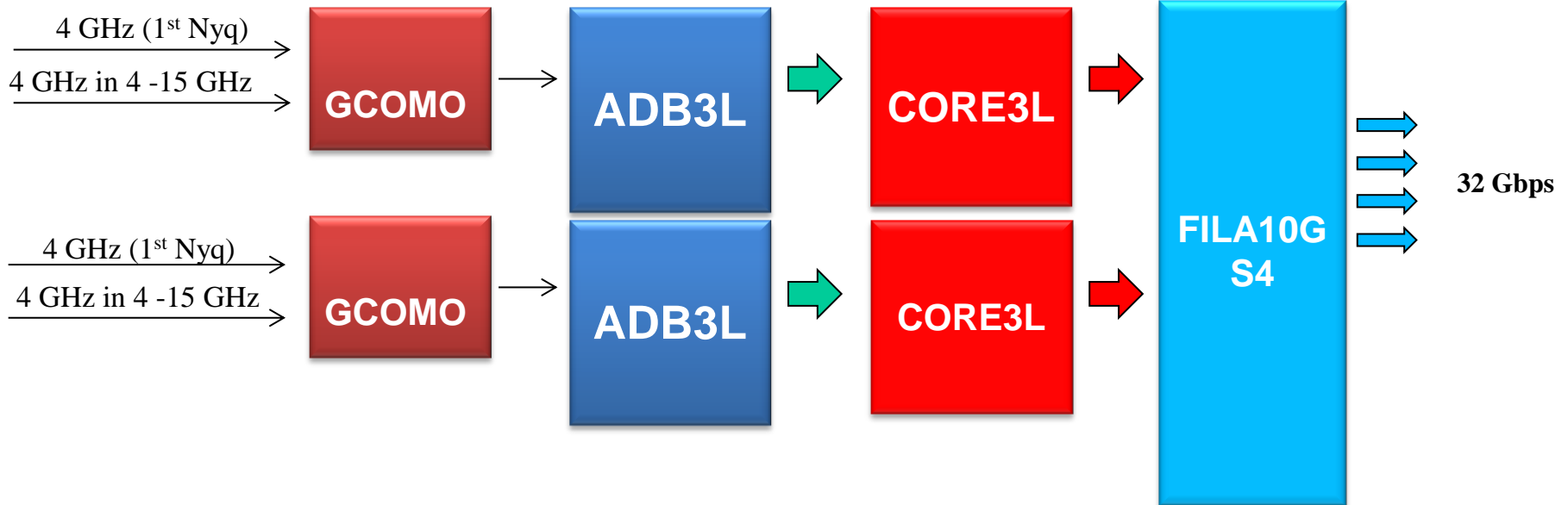
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CORE3H

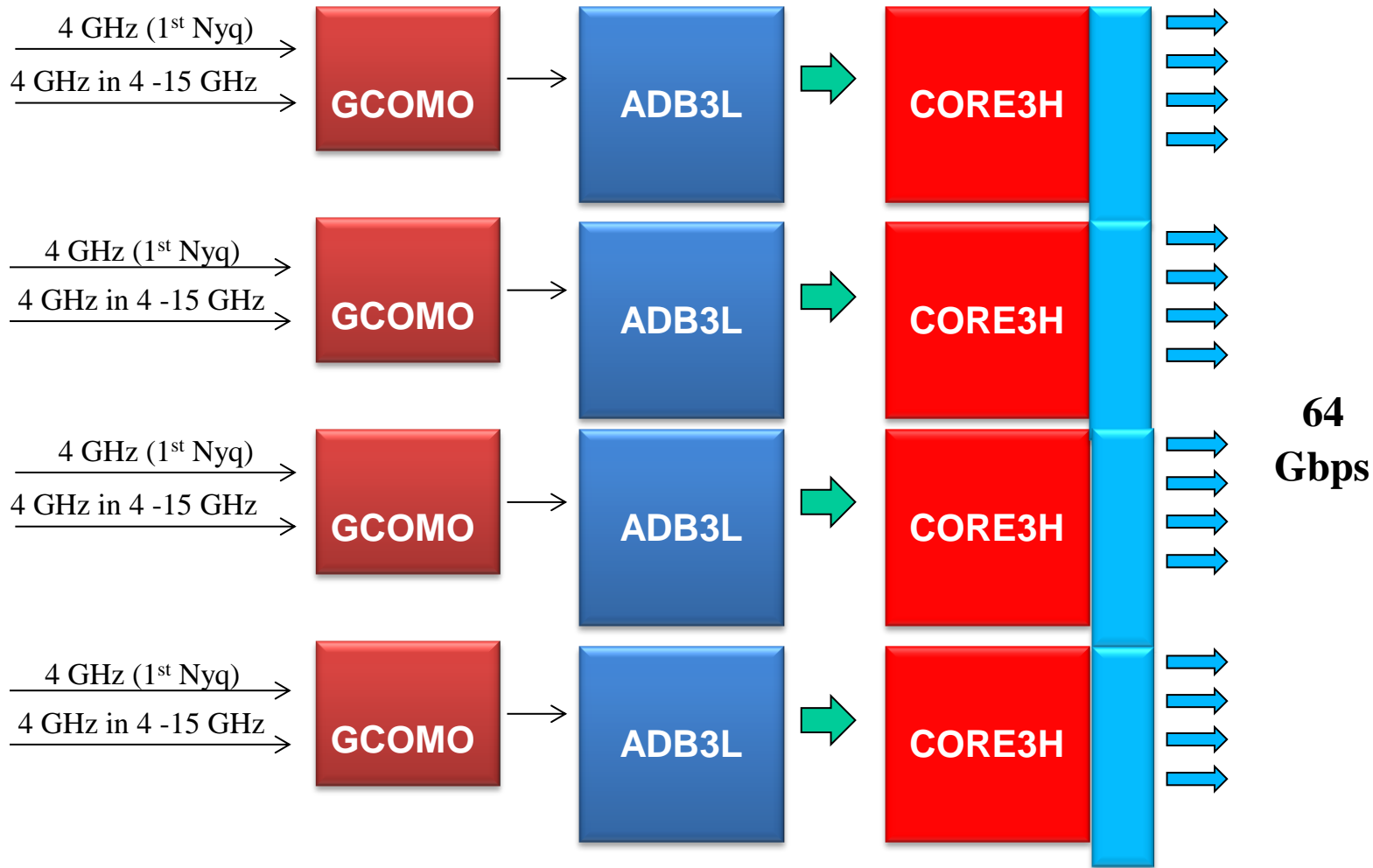


- Input bus: **HSI & HSI2**
- Input sampling representation: **8-10 bit**
- Input bandwidth : 1 x **4GHz**, 2 x **2GHz**, 4 x **1GHz**
- Processing capability: **DDC, PFB, DCS**
- Output: **8 x 10GE SFP+**
- Inter-board bus: **8 Input 10GE SFP+**
- Compatibility with existing DBBC environment

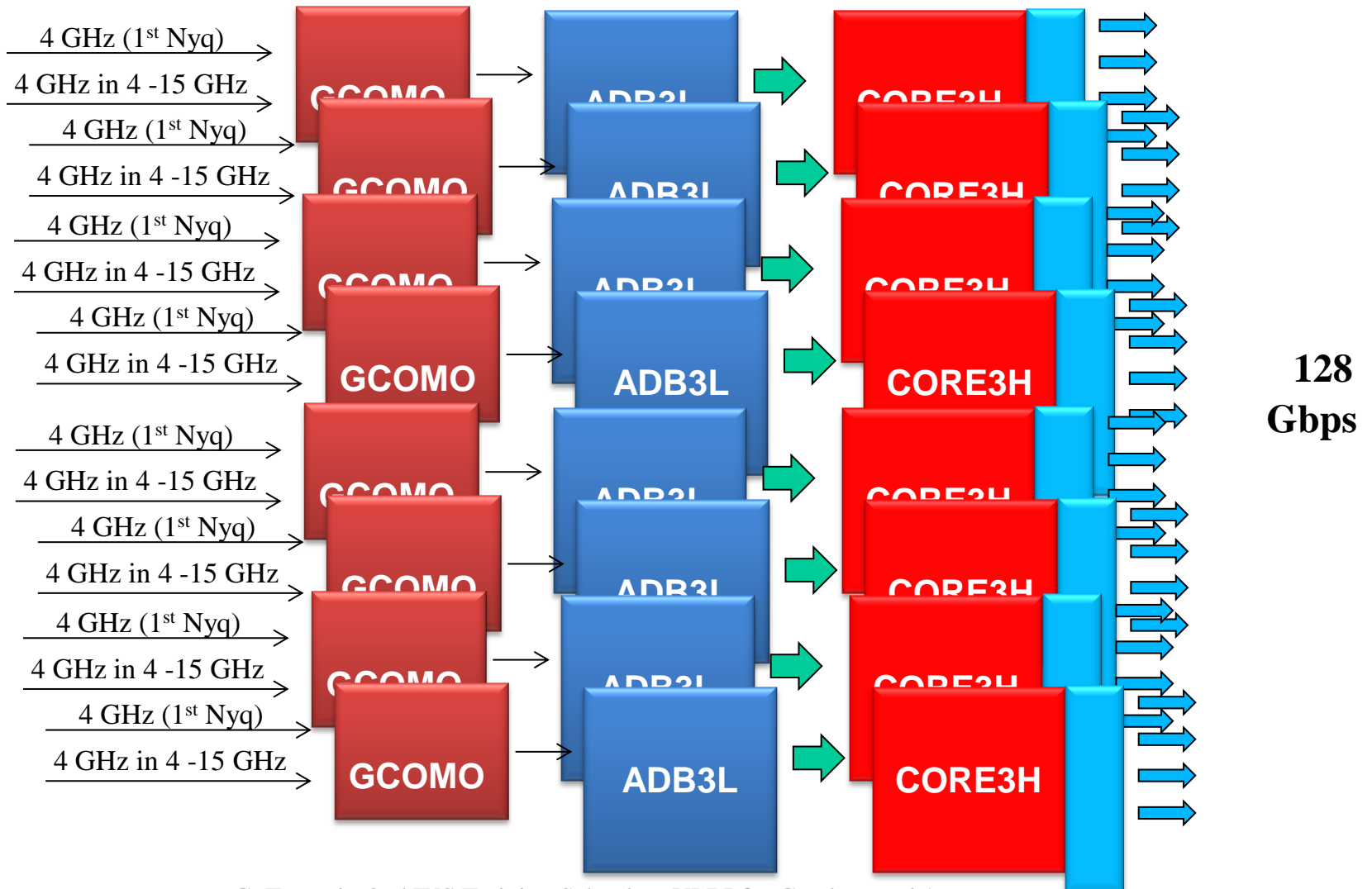
DBBC3L-2L2L Architecture

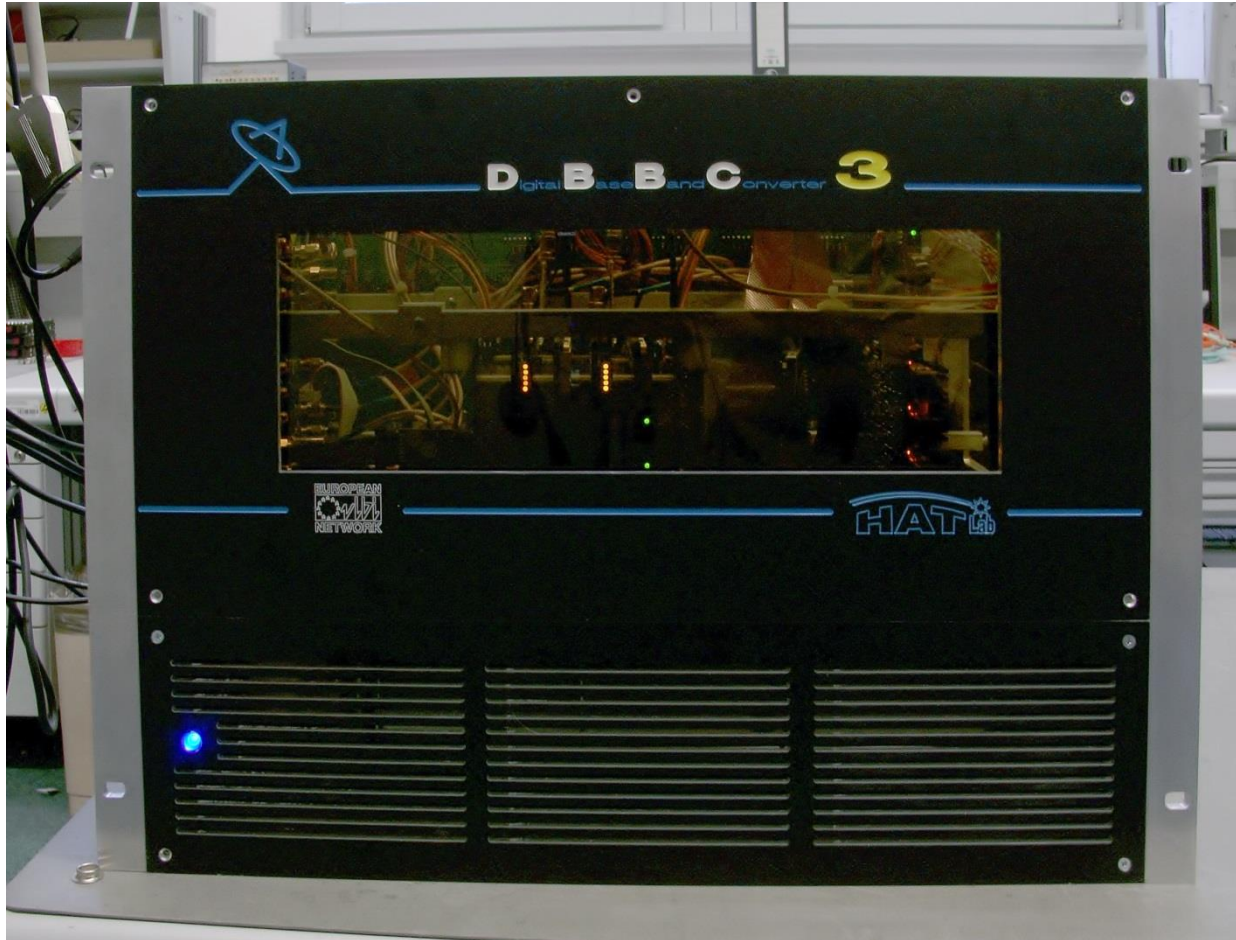


DBBC3L-4L4H Architecture



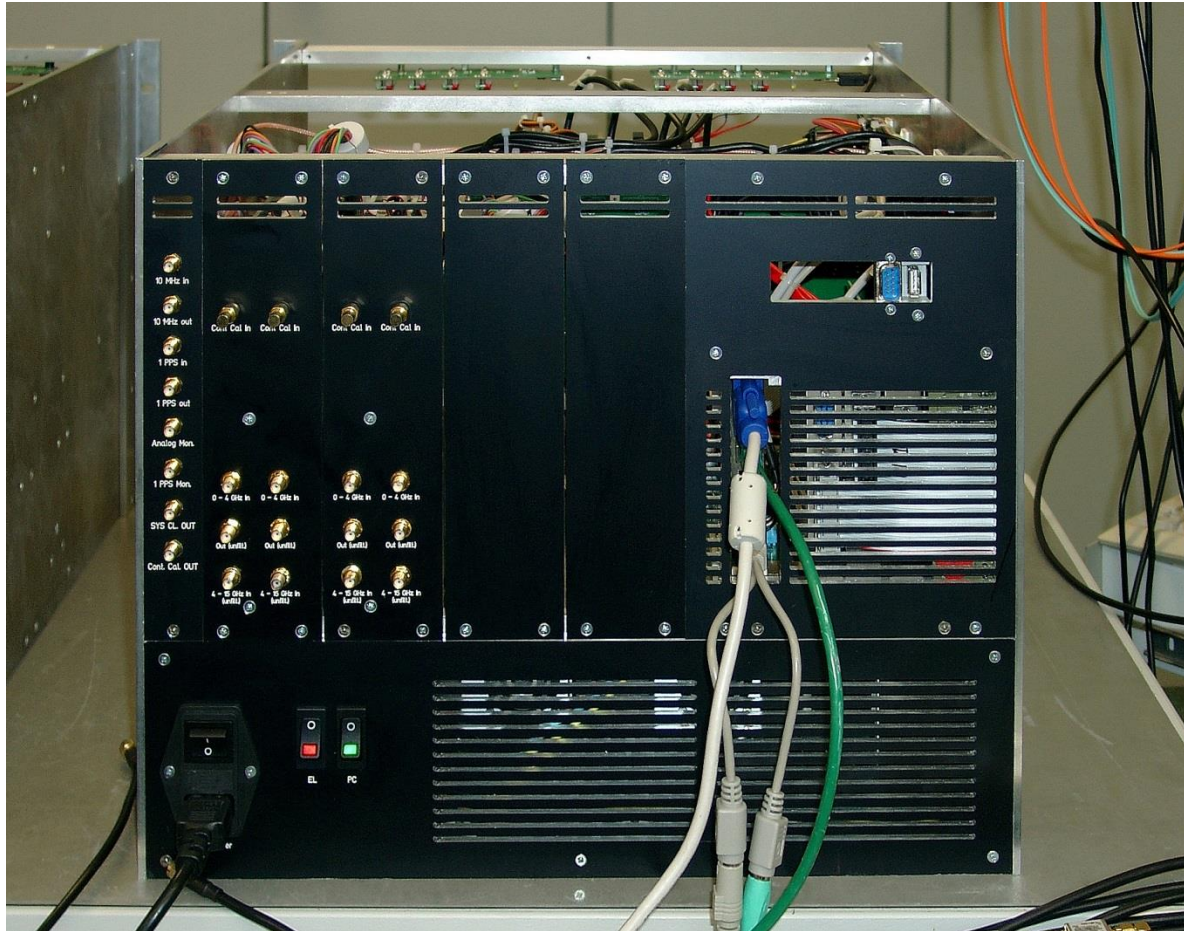
DBBC3L-8L8H Architecture





DBBC3L front view

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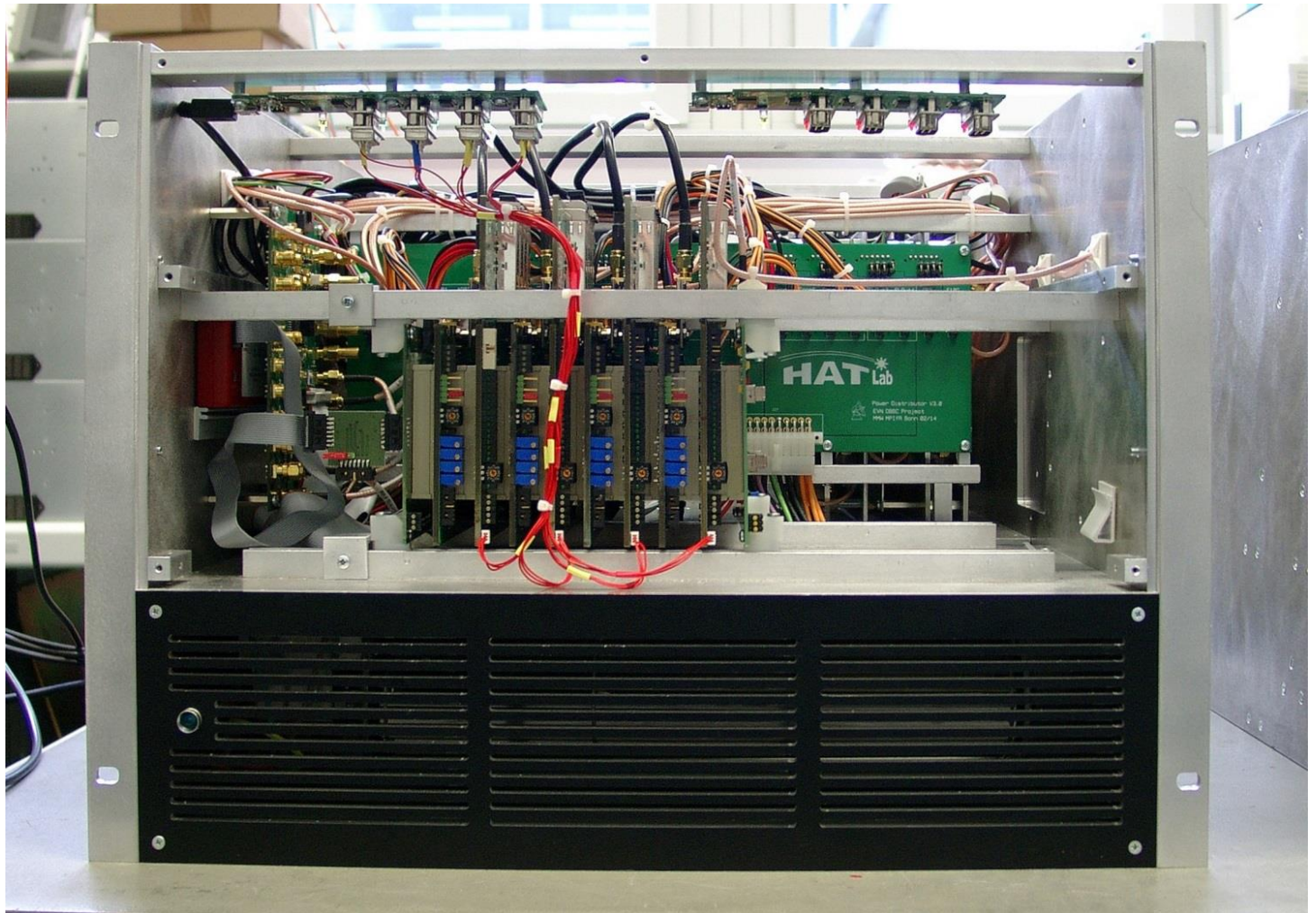
DBBC3L rear view

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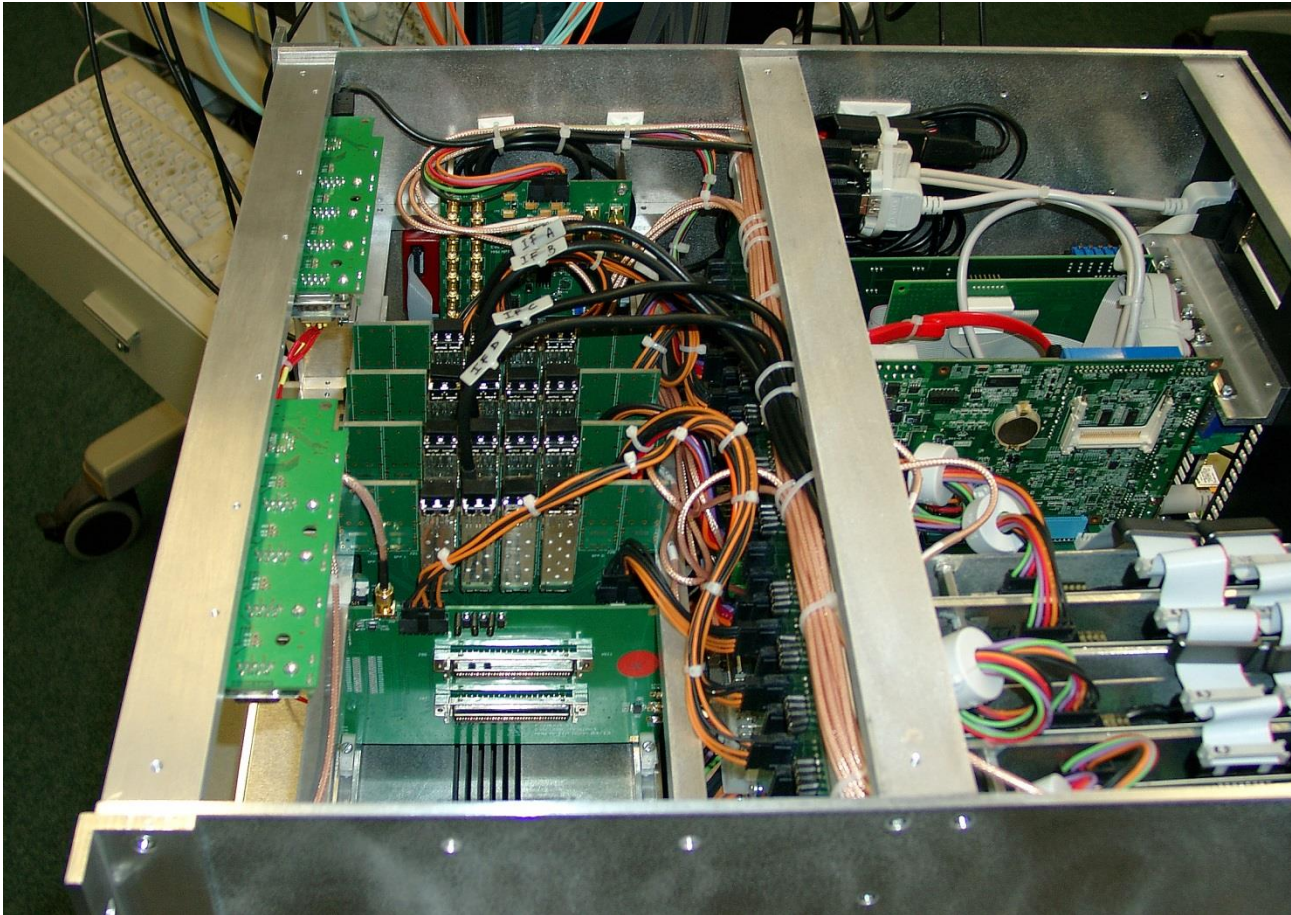


DBBC3L
with CORE3L
and FILA10G-S4

DBBC3L
with CORE3H



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DBBC3L top view with CORE3H

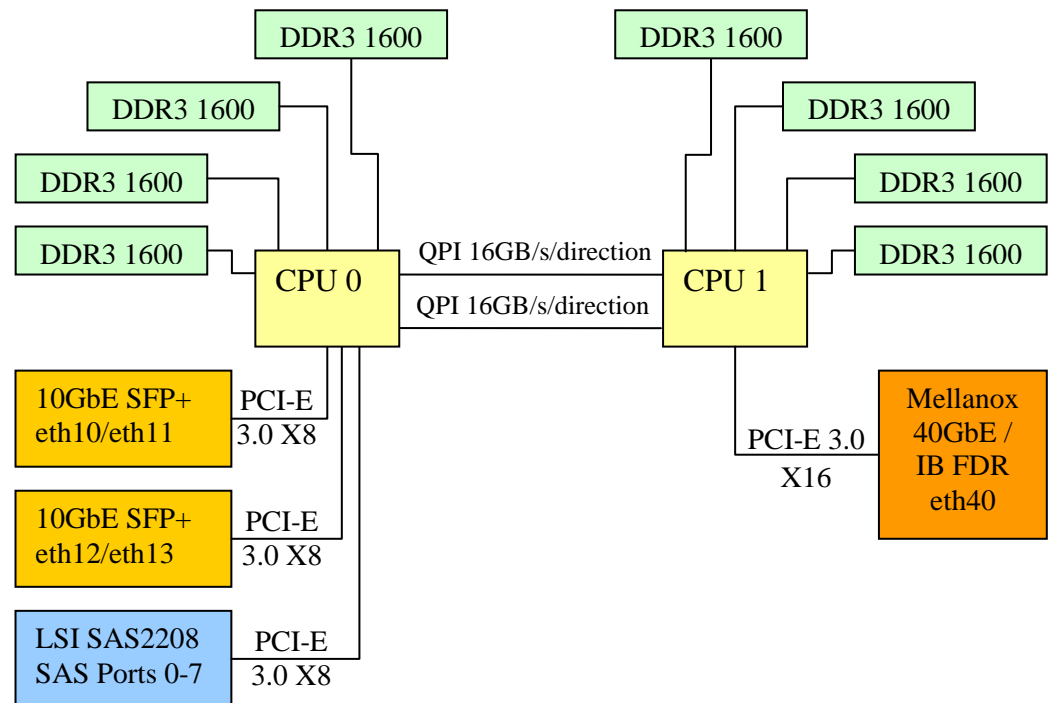
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FILA40G General Key features

- 4 x 10GE Inputs / module
- 1 x 40GE Output / module
- Stream aggregation (2/4 threads are cumulated in single thread)
- Format conversion/VDIF threading
- Packet filtering
- Pulsar gating
- Timekeeping via NTP and/or GPS module
 - Propagates UTC to other connected devices via DBBC Local Network (DLN)
- Optional disk storage
 - Expected to record at 32Gbps sustained / module
 - Compatibility with Mark6 disk packs/chassis being investigated

FILA40G Architecture for 32 Gbps

- 2 x Intel Xeon E5-2670
 - 8 core 2.60 GHz
- 8 x 8GB DDR3 1600
- 8 Onboard SAS2 ports
- 4 free PCI 3.0 x8 slots
 - To be used to add extra SAS2/3 ports



Status FILA40G 3 systems assembled + 40G Protocol Analyzer available (MPI)



DBBC2 DDC Control Commands

Standard main commands

DBBCnn = freq, IF, bwd, TPint

where

nn => 01, .. ,16 indicates the number of bbc;

freq => is the base band frequency in MHz, in the range 0010.000000 - 3,072.000000;

IF => A or B or C or D. Any Core2 is connected to a band in the standard communication so this value is only informative.

bwd => bandwidth of both sidebands, 1-2-4-8-16MHz base version, 2-4-8-16-32MHz E and F versions;

tpint => tp integration time, in seconds

DBBC2 DDC Control Commands

DBBCIF(A,B,C,D) = input_ch, attenuation, filter, target_agc, update_time

where

input_ch => input channel of the four possible (1,2,3,4) .

attenuation => the gain of the channel is set in manual mode if a number is indicated in the range 0 - 32 dB, step 0.5 dB. If AGC is indicated the gain is automatically set so to satisfy the optimal level for the analog to digital converter. If MAN is indicated automatic gain control is stopped.

filter=> 2 (10-512 MHz), 1 (512-1024 MHz), 4 (1024-1536 MHz), 3 (1536-2048 MHz)
6 (0-1024 MHz), 5 (L band), 8 (ext 1), 7 (ext 2)

target_agc=> value for the AGC (0-65535)

update_time=> time interval for update gain parameter in agc

DBBC2 DDC Control Commands

DBBCFORM = VSI mode

VSI mode => is the mapping of the 64 channels in the VSI1/2 interfaces. Possible predefined values are: GEO, ASTRO, ASTRO2, WASTRO, TEST, LBA, 8bit.

If TEST is indicated an addition parameter is needed: 0 all VSI output are set to 0, 1 all VSI output are set to 1, tvg VSI output contain mk5b test vector, bin VSI output contain binary counter.

8bit mode is available in v105 only. A preliminary selection of which USB or LSB of one of the four bbc available to send to the output is necessary. Only one bbc per group available in a Core2 can be selected. The selection is done with

reg=bbc#,3,sideband

bbc#=>1|2|3|4 in Core2#1, 5|6|7|8 in Core2#2, 9|10|11|12 in Core2#3, 13|14|15|16 in Core2#4

sideband=>2 for USB, 3 for LSB

DBBC2 DDC Control Commands

PPS_SYNC

Synchronize to the external 1pps

DBBCGAIN=dbbcnn, second parameter,third parameter

Set the system gain level and set the power level after down-conversion.

dbbcnn => 1, 2, .., 16, all

second parameter => gainU as 1, .., 255, step 1

agc, set a same TP value for USB and LSB

as defined in the third parameter

man, freeze the present gain value

third parameter => gainL as 1, .., 255, step 1

total power target if the second parameter is 'agc'

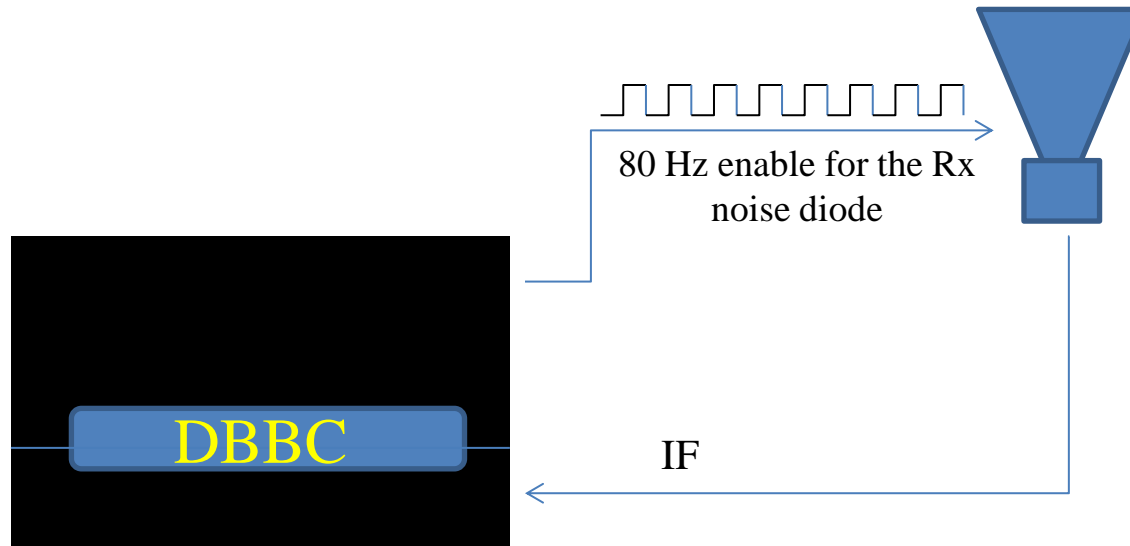
in the range 0-65535

CONT_CAL = status

Continuous calibration noise diode activation at 80 Hz rate.

status => on | off

80 Hz Continuous Noise Calibration



cont_cal=off

dbbc01= 567.99,a,8,1,agc,10,10,3480,3628,0,0

dbbc02= 715.99,a,8,1,agc,10,10,3129,2997,0,0

cont_cal=on

dbbc01= 567.99,a,8,1,agc,10,10,1860,1929,1615,1703

dbbc02= 715.99,a,8,1,agc,10,10,1693,1586,1421,1412

DBBC2 PFB Control Commands

Standard main commands

power = nn

total power reading for a bank of 15 adjacent channels as produced by a single Core2

nn => 1, .. ,4 indicates the board number;

Reports the total power values for all the bbcs in a PFB and as last indication a flag (0|1) indicating a possible overflow status (1) in the channel group.


dbbcif(a|b|c|d) = input_ch, attenuation, filter, target_agc_value, update_time

as it was in DDC

DBBC2 PFB Control Commands

dbbcform = form,[test_mode]

Set the output format:

form = spol => single pol output 

form=dpolc => dual pol contiguous

form=dpolm => dual pol mirror

form=dpoli => dual pol interleaved

form=full => full band (DSC) 

form=byp => bypass

form=full => flex 

form= copy => copy VSI1 on VSI2

form=test,0 => test mode all 0

form=test,0 => test mode all 1

form=test,bin => test mode binary counter

form=test,tvg => test mode TVG

DBBC2 PFB Control Commands

Dbbctrk1(2) =nn,source-ch, source-ch, ... ,source-ch

Set the output data channel assignment in VSI1(2)

nn => Core2 board to be set

then 16 fields follow defining the content of the 16 VSI ordered output channels

source =>

p for PFB pattern coming from the same board

v1 for the pattern coming from the input VSI1 to the Core2

v2 for the pattern coming from the input VSI2 to the Core2

ch => the channel number (including sign and magnitude) coming with p,v1,v2

FILA10G Control Commands

Physical data input selection

inputselect

Selects one of the available input data sources.

Arguments: <input source>

<input source>: valid values are: (tvg|vsi1|vsi2|vsi1-2|vsi1-2-3-4)

FiLa10G's physical input width is 128 bit wide.

vsi_samplerate

Gets or sets the VSI input sample rate (samples per second).

Arguments: [<#samples per second> [<decimation divisor>]]

<#samples per second> (optional): lets the system know the sample rate of the VSI input (samples per second)

<decimation divisor> (optional): a divisor d in the range 1..255.

$d=1$ is the default, i.e. no decimation. $d>1$ decimates the input such that the resulting sample rate is $1/d$ of the original rate.

All arguments are optional. If the command is called without arguments the current VSI input sample rate is displayed.

FILA10G Control Commands

Selection of data from the physical input

vsi_bitmask

Gets or sets the VSI input bitmask.

Arguments: [[[[<bitmask-4>] <bitmask-3>] <bitmask-2>] <bitmask-1> |reset]

<bitmask-X> (optional): a 32 bit bitmask each, that specifies the active bits of VSI-X.

Omitted bitmasks are assumed to be zero (0x00000000). The only rule for the values is that in total at least one bit must be active.

All arguments are optional. If the command is called without arguments the current VSI bitmask is displayed.

The up to four 32 bit wide bitmasks specify which bits of a VSI input stream are active and being processed, the others are discarded. This effectively reduces the data amount.

If the command is called with the "reset" argument, all of the bitmasks are reset to their default value (0xffffffff = all active).

In general, the number of active bits in the bitmask should be a power of two (1,2,4,8,16,32,64,128).

If the number of active bits is not a power of two, the highest active bit is replicated in the resulting data word until the the next power of two is reached. This special case is displayed as a warning by the command.

FILA10G Control Commands

Decimation of data input

vsi_inputwidth

Gets or sets the effective bit width of the VSI input, that is to be processed by FiLa10G.

Arguments: [<input width in bits>]

<input width in bits> (optional): allowed input widths: 1,2,4,8,16,32,64,128

If the command is called without arguments the current input width is displayed. Otherwise the input width is set to the new value.

FiLa10G has a 128 bit wide input width, such that up to 128 parallel input bit streams are supported.

Only the <input width in bits> bit streams with the lowest index are fed to the processing pipeline.

The internal data path width of FiLa10G is 64 bit. Input widths lower than 64 result in the input data being packed to the internal data path width. An input width of 128 will result in the input data being serialized to two consecutive 64 bit words.

When a VSI input is selected ("inputselect"), the input width is automatically set to the actual size of the selected input.

Note: In general, the input width should be equal to or lower than the width of the actual VSI input source. Higher input widths will likely waste memory on the recorder.

Note: multi-channel VDIF format is only supported for the input widths 32 and 64.

Note: the "VSI input width" is also modified by the command "vsi_bitmask". Thus, using a custom bitmask and a custom input width at the same time may lead to unexpected results.

FILA10G Control Commands

Operational status set and Data format

reboot

Reboots the system.

FiLa10G's hardware and software is reset to its initial state, i.e. as it was directly after the programming of the FPGA, and lets the FiLa10G system boot again.

Warning: all previously done settings and states are lost when rebooting.

reset

Resets FiLa10G's datapath and erases synchronized time.

Arguments: [keepsync]

If "reset" is called without arguments, the complete data path is reset and time synchronization is lost.

If "reset" is called with argument "keepsync", FiLa10G tries to maintain the current time synchronization. For this to work the input stage of the data path and the timers are not reset.

start

Starts/restarts sending of (formatted) output data.

Arguments [(vdif|mk5b|raw) [force]]

The used output data format is either VDIF, Mark5B or raw format. Raw format requires no time synchronization. The VDIF and Mark5B formats require the respective timer to be set.

stop

Stops sending of output data (the opposite of "start").

FILA10G Control Commands

Physical data output

vsi_outputselect

Selects the VSI output data source.

Arguments: [<output data source>]

<output data source> (optional): (vsi1-2|vsi<X>-<Y>|output<X>|eth<X>|eth<X>-data)

If the command is called without arguments the current VSI pack mode is displayed.

The data that appears at the VSI outputs can be configured by the user. By default the VSI-1 input is connected to VSI-1 output and VSI-2 input is connected to VSI-2 output.

The following sources are available:

- **vsi1-2**: the default output
- **vsi1-1**: both VSI outputs are connected to VSI-1
- **vsi2-2**: both VSI outputs are connected to VSI-2
- **vsi2-1**: like the default, but having VSI-1 and VSI-2 flipped
- **output0**: VSI-1 output is connected to the lower 32 bits of the data stream at output 0 of the FiLa10G core. VSI-2 output is connected to the respective higher 32 bits.
- **output1**: VSI-1 output is connected to the lower 32 bits of the data stream at output 1 of the FiLa10G core. VSI-2 output is connected to the respective higher 32 bits.
- **eth0**: VSI-1 output is connected to the lower 32 bits of the data stream received from Ethernet core "eth0". VSI-2 output is connected to the respective higher 32 bits.
- **eth1**: VSI-1 output is connected to the lower 32 bits of the data stream received from Ethernet core "eth1". VSI-2 output is connected to the respective higher 32 bits.

Physical data output (continue)

.....vsi_outputselect

- **eth0-data:** same as "eth0" with the difference that all VDIF and Mark5B header data is cut from the incoming data stream.
- **eth1-data:** same as "eth0" with the difference that all VDIF and Mark5B header data is cut from the incoming data stream.

The PPS signal can be reconstructed correctly from the packet stream being received over Ethernet, if the packet format can be recognized and the packets are well-formed and arrive in sequential order. The stream received from an Ethernet source is recognized as Mark5B data if the incoming packet size is exactly 5008 bytes and the used sync word equals 0xabaddeed. It is interpreted as Raw data if the packet size is exactly 8192 bytes, which disables any further header analysis and especially the PPS signal reconstruction feature. It is interpreted as VDIF data in any other case.

Applies to VDIF and Mark5B format only: The PPS signal is reconstructed and attached to the output stream whenever the first packet in a second interval is detected (see respective standard for details). Note: the VSI output uses the same clock as the selected source. This is either the current system clock or the clock from the VSI input ports.

FILA10G Control Commands

Parameters in the data format

vdif_frame

Gets or sets the properties of VDIF frames.

Arguments: [<channel bit width> <#channels per frame> [<payload size in bytes>]]

<channel bit width> (optional): the size of each channel in bits (allowed values: 1,2,4,8,16,32,64)

<#channels per frame> (optional): number of channels per VDIF frame (allowed values: 1,2,4,8,16,32,64,128)

<payload size in bytes> (optional): the total payload size (= frame size without header data) of the VDIF frames.

All arguments are optional. If the command is called without arguments, the properties are not modified but only displayed.

If successful, the command displays the resulting number of frames per second and the number of data threads, according to the currently selected input. A warning is displayed instead if the VDIF frame properties do not match the currently selected input.

Note: after having set the VDIF frame properties and when processing has already been started, a reset of the datapath (i.e. "reset" or "reset keepsync") is mandatory.

Following rules apply to the properties:

1. The width of a data sample in a frame (<sample bit width>) equals to <#channels per frame> * <channel bit width> bits.
2. <sample bit width> must be 128 or less
3. If one of the properties is set and <payload size in bytes> is omitted, the optimal payload size is computed for the currently selected input.

FILA10G Control Commands

Parameters in the data format (continue)

.....vdif_frame

4. Setting an "illegal" payload size is allowed but with the following restrictions:

- a) If a <payload size in bytes> is given that exceeds the maximum supported payload size for this configuration, the payload size is automatically capped to the maximum
- b) If <payload size in bytes> will result in the last frame of a second interval to be incomplete, this frame is silently discarded.

vdif_interval

Gets/sets the active frame ID interval within a 1PPS period.

Arguments: [<minimum frame ID> <maximum frame ID>]

<minimum frame ID> (optional): the minimum frame ID that is transmitted to the output.

allowed range: 0...4294967294

<maximum frame ID> (optional): the maximum frame ID that is transmitted to the output.

allowed range: 0...4294967295

"*" is a shortcut for maximum frame ID.

Frames are filtered by their ID, such that only frame with an ID in the range <minimum frame ID> to <maximum frame ID> appear in the output stream. The others are completely discarded from the stream.

The frame index starts with 0 for the first VDIF frame in the second interval. The frame index increases with each following VDIF frame until it restarts again with 0 for the first frame of the next second interval.

Execute "vdif_interval 0 *" to reset the interval setting to its standard value.

Note: the frame ID interval setting applies to the VDIF data format only.

FILA10G Control Commands

Parameters in the data format (continue)

vdif_leapsecs

Gets/sets the number of UTC leap seconds since VDIF reference epoch.

Arguments: [<leap seconds>]

<leap seconds>: the number of additional leap seconds since VDIF reference epoch (optional)

Generally, the number of leap seconds since the start of the VDIF reference epoch is zero, since UTC leap seconds are inserted at the end of a half-year and the reference epoch is set to the beginning of the current half-year.

This command exists for the case in which a UTC leap second needs to be inserted between the beginning of the reference epoch and the current time. With this command the user can manually insert any number of missing leap seconds. Furthermore, a negative leap second number allows the removal of seconds relative to the start of epoch.

vdif_legacy

Enables (on) or disables (off) VDIF legacy headers.

Arguments: (on|off)

Note: setting this value directly affects the header data of the VDIF data format.

vdif_station

Gets/sets the VDIF station ID.

Arguments: [<VDIF station ID>]

<VDIF station ID> (optional): a two character VDIF station ID (cmp. VDIF standard)

Note: setting this value directly affects the header data of the VDIF data format.

Time synchronization

mk5b_timesync

Performs Mark5B time synchronization to the active 1PPS source.

Arguments: <years since 2000> <modified Julian day> <seconds>

<years since 2000>: the number of years since 2000 (=currentYear-2000)

<modified Julian day>: the current modified Julian day (only the last three digits are required)

<seconds>: the past seconds within the current modified Julian day.

A valid PPS signal is required for the time synchronization to succeed. If successful, the Mark5B time is synchronized with this command.

vdif_timesync

Performs VDIF time synchronization to the active 1PPS source.

Arguments: <half years since 2000> <seconds>

<half years since 2000>: the number of past half years since 2000 (only complete half years are counted)

<seconds>: the number of seconds since the beginning of the current half year

A valid PPS signal is required for the time synchronization to succeed. If successful, the VDIF time is synchronized with this command.

FILA10G Control Commands

Time synchronization (continue)

timesync

Performs time synchronization to the active 1PPS source.

Arguments: <YYYY>-<MM>-<DD>T<hh>:<mm>:<ss>[(+|-)<ZZ:ZZ>]

<YYYY>: the current year in four digit representation (range: 2000..2130).

<MM>: the current month (range: 1..12)

<DD>: the current day (range: 1..31)

<hh>: the current hour (range: 0..23)

<mm>: the current minute (range: 1..59)

<ss>: the current second (range: 1..59)

(+|-)<ZZ:ZZ>: the time zone offset (only full hours are supported)

the offset is optional. if omitted offset 00:00 (=GMT) is the default.

(Example time: 2013-07-09T15:41:33+01:00)

A valid PPS signal is required for the time synchronization to succeed. If successful, both VDIF time and Mark5B time are synchronized by this command.

FILA10G Control Commands

Ethernet settings

arp

Enables (on) or disables (off) ARP queries on both Ethernet cores (eth0 and eth1).

Arguments: (on|off)

destination

Gets/sets the output destination.

Arguments: <output index> [(<IPv4 address>[:<port>]|none) [<thread ID>]]

<output index>: the index of the output for which the destination is to be got or set.

allowed values: 0, or 1

<IPv4 address>(optional): IP address, format x.x.x.x

<port>(optional): IP port number

<thread ID>(optional): specifies the ID of the data thread for which the destination is to be set

Execute the command in the form "destination <output index>" to get a list of all current destination settings for the respective output.

tengbarp

Sets one ARP entry in a 10Gb Ethernet device.

Arguments: <device name> <ARP table index> <MAC address>

<device name>: "eth0", or "eth1"

<ARP table index>: index of ARP table entry to be modified

<MAC address>: MAC address to be set

FILA10G Control Commands

Ethernet settings (continue)

tengbcfg

Sets the parameters of a 10Gb Ethernet device.

Arguments: <device name> <tengbcfg parameters>

<device name>: "eth0", or "eth1"

<tengbcfg parameters>: the parameters to be set

tengbinfo

Retrieves the current parameters of a 10Gb Ethernet device.

Arguments: <device name>

<device name>: "eth0", or "eth1"

FILA10G Control Commands

Status monitoring

output

Displays output debug information.

Arguments: [<output index> [<frame ID> [<duration>]]]

<output index>: 0 or 1 (in current implementation both outputs send same data)

<frame ID>: Index of frame within current second starting with 0.

sysstat

Displays information about the current status of the system and gives an overview of the state of the most important user settings.

tick

Enables (on) or disables (off) continuous 1PPS tick display on the console.

Arguments: (on|off)

Note: for compatibility to legacy batch scripts "tick" may be called without arguments which toggles the state between "on" and "off".

time

Displays the current time of the active 1PPS source.

Arguments: –

The displayed time is the (synchronized) VDIF time in UTC format.

version

Displays the version of the firmware (distinguishing between hardware and software version)

FILA10G Control Commands

Testing mode

tvg_mode

Gets or sets the test vector generator mode.

Arguments: [<tvg mode>]

<tvg mode> (optional): valid values are: (all-0|all-1|vsi-h|cnt)

If the command is called without arguments the current TVG mode is displayed.

tvg_samplerate

Gets or sets the TVG sample rate (samples per second).

Arguments: [<#samples per second>]

<#samples per second> (optional): sets the sample rate (samples per second) of the TVG input.

Valid range is: 1...64000000

Note: the TVG is operated with a 64MHz clock.

FILA10G Control Commands

Web pages

FiLa10G Configuration

Home > FiLa10G Configuration

FiLa10G Configuration

Display # 20

1	FiLa10G Configuration v3.3.2	424
2	FiLa10G Configuration	335
3	FiLa10G - S4 Configuration	287

search...

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Time Correction: +/-0..60s (requires user interaction on console)

5. Output Format

Data Format: Output 0: VDIF, Output 1: VDIF

VDIF Settings: Corner Turning: on, VDIF Encoding: standard

VDIF Frame Setup: Channel Width, Channels per Frame, Payload Size, # Threads, Station ID, Extended User Data

FiLa10G Commands

```
reboot
# Input Configuration
splitmode off
inputselect tvg
tvg_mode vsi-h
vsi_samplerate 64000000
reset
# Time Synchronization
timesync
# Output Configuration
vdif_frame 2 16
vdif_station na
destination 0 192.168.1.2:46227
destination 1 192.168.1.3:46227
vsi_outputselect vsi1-2
start vdif
```

6. Ethernet Output

Destination Addresses: Enter IPv4 destination address and port of client (note: for no destination (=output disabled):

Output 0: 192.168.1.2:46227

Output 1: 192.168.1.3:46227

7. VSI Output

Data Source: VSI-1-2

Generate FiLa10G Commands