L06: How do we sample data? Digital backends

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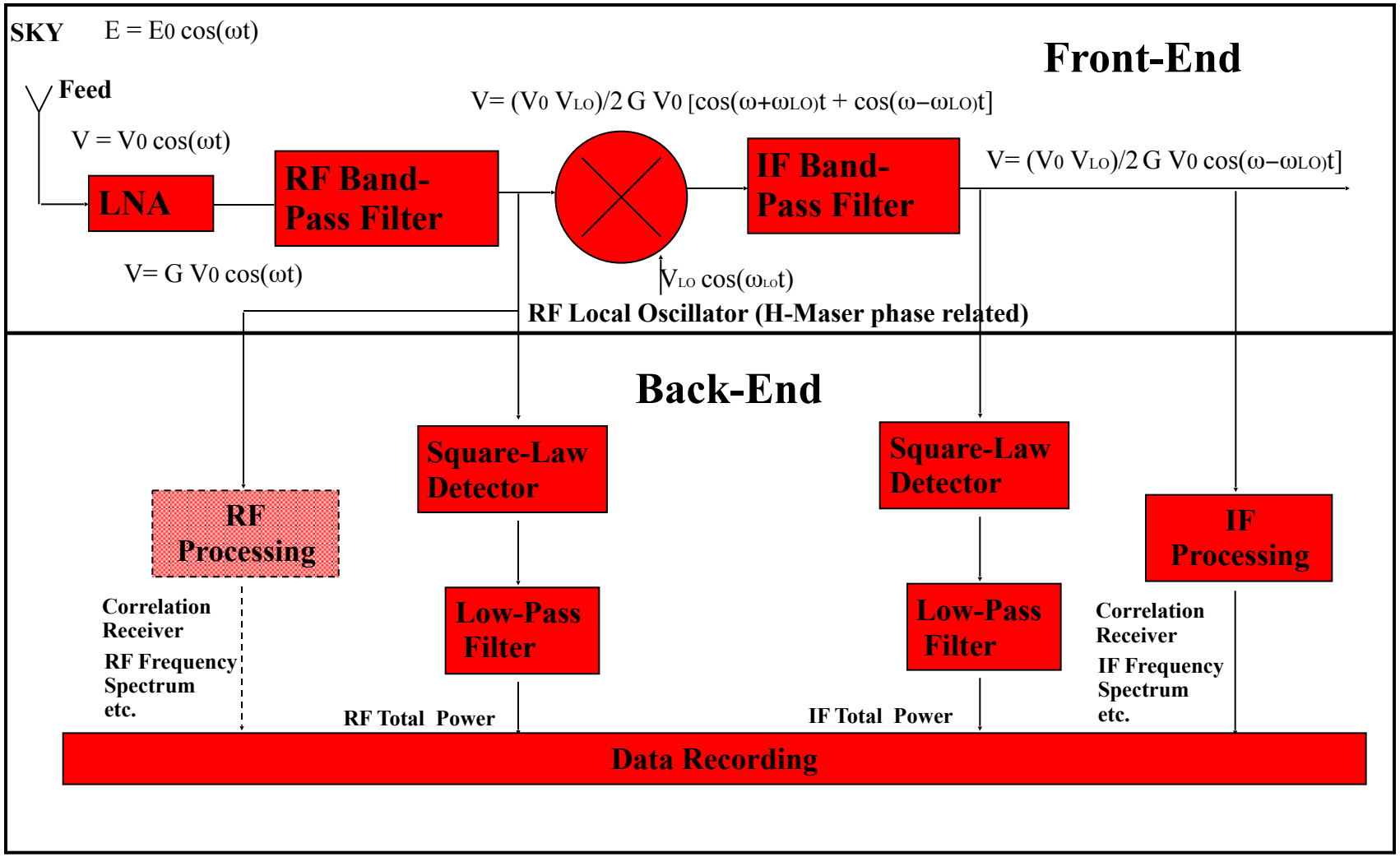
Overview

- General functionality of a VLBI signal chain
- Some theoretical concepts as background
- Digital Backend
- Operating modes: DDC / PFB / DSC
- DBBC generations

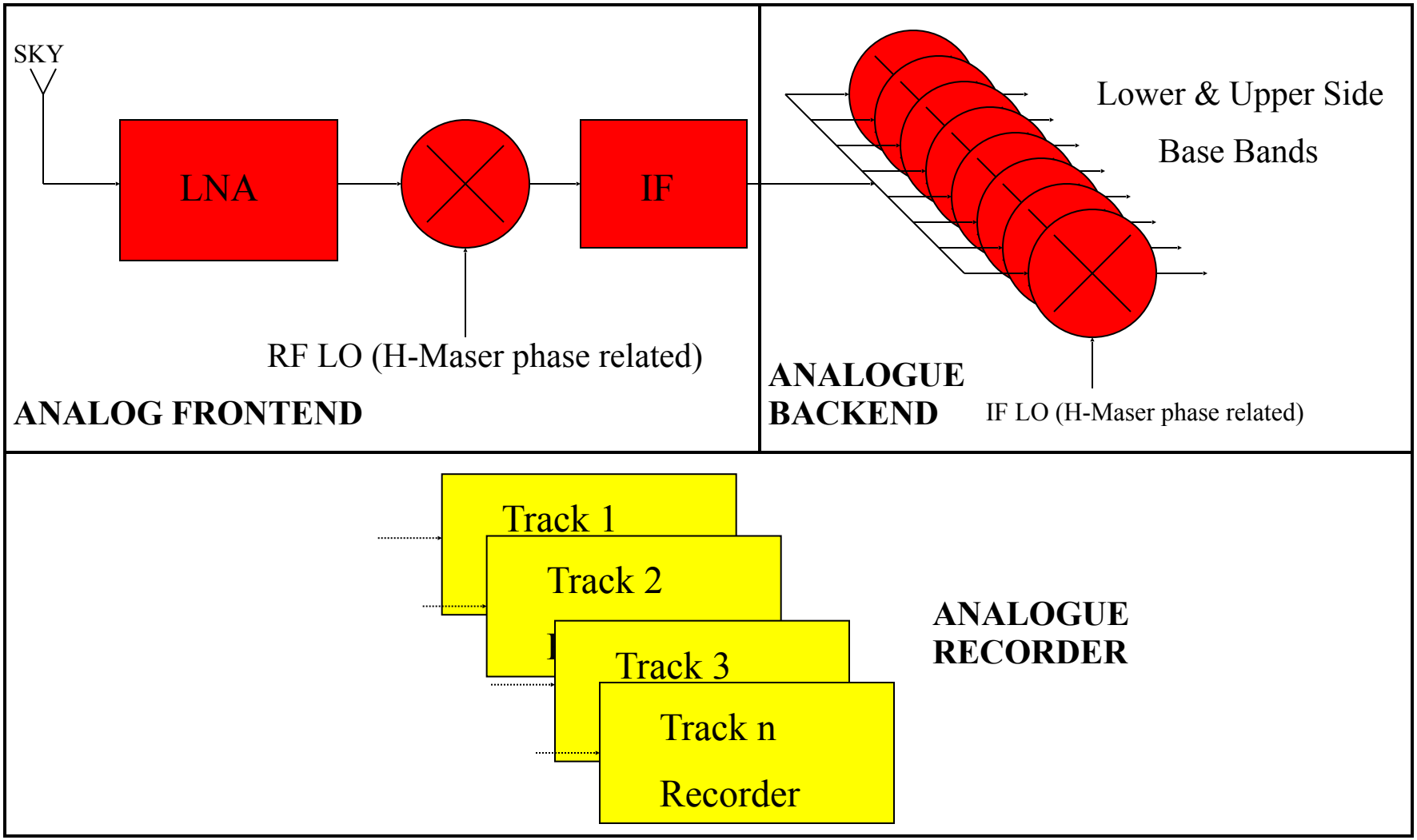
General Functionality
VLBI Signal Chain Schematic Block

VLBI Signal Chain in more detail

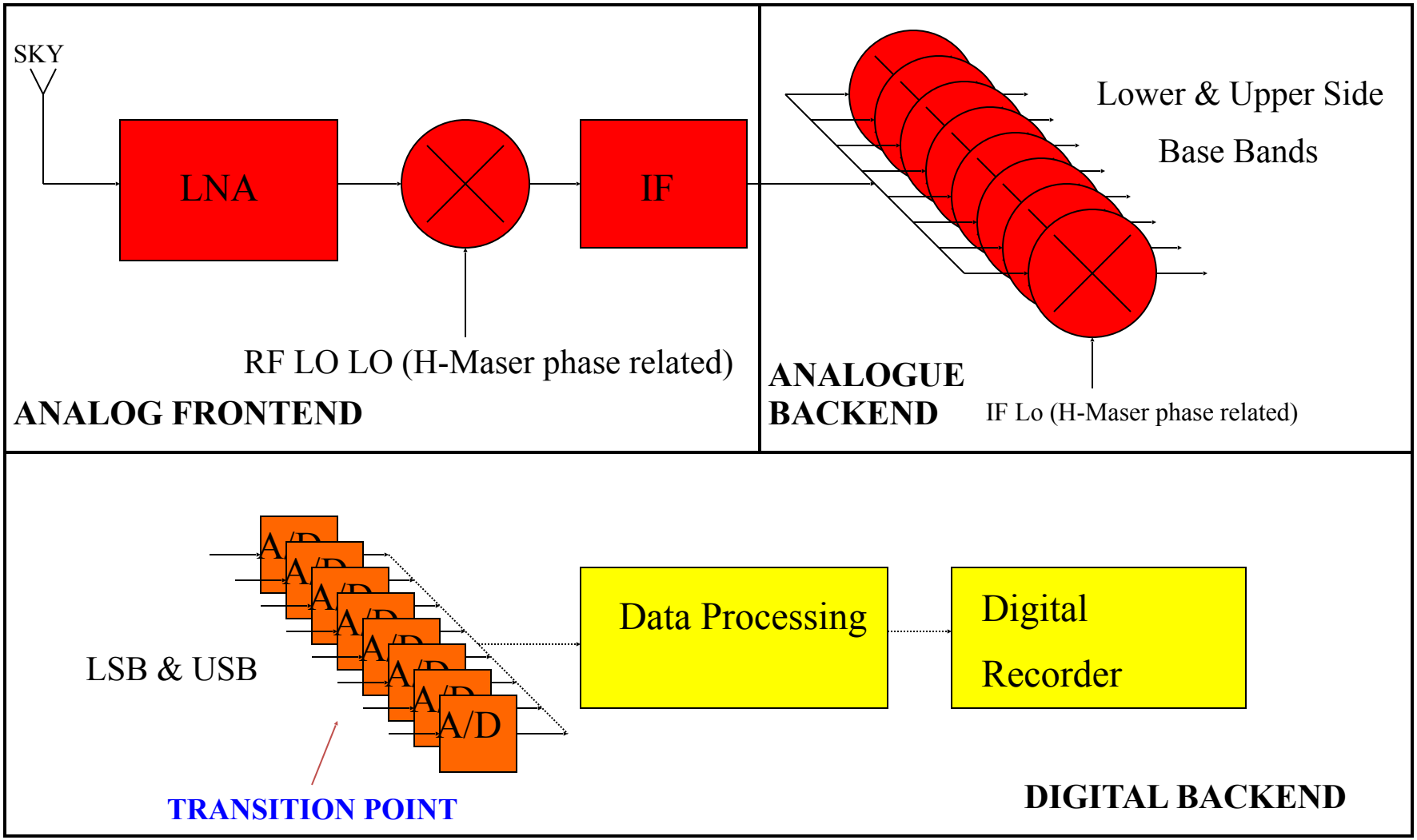


From Analogue to Digital

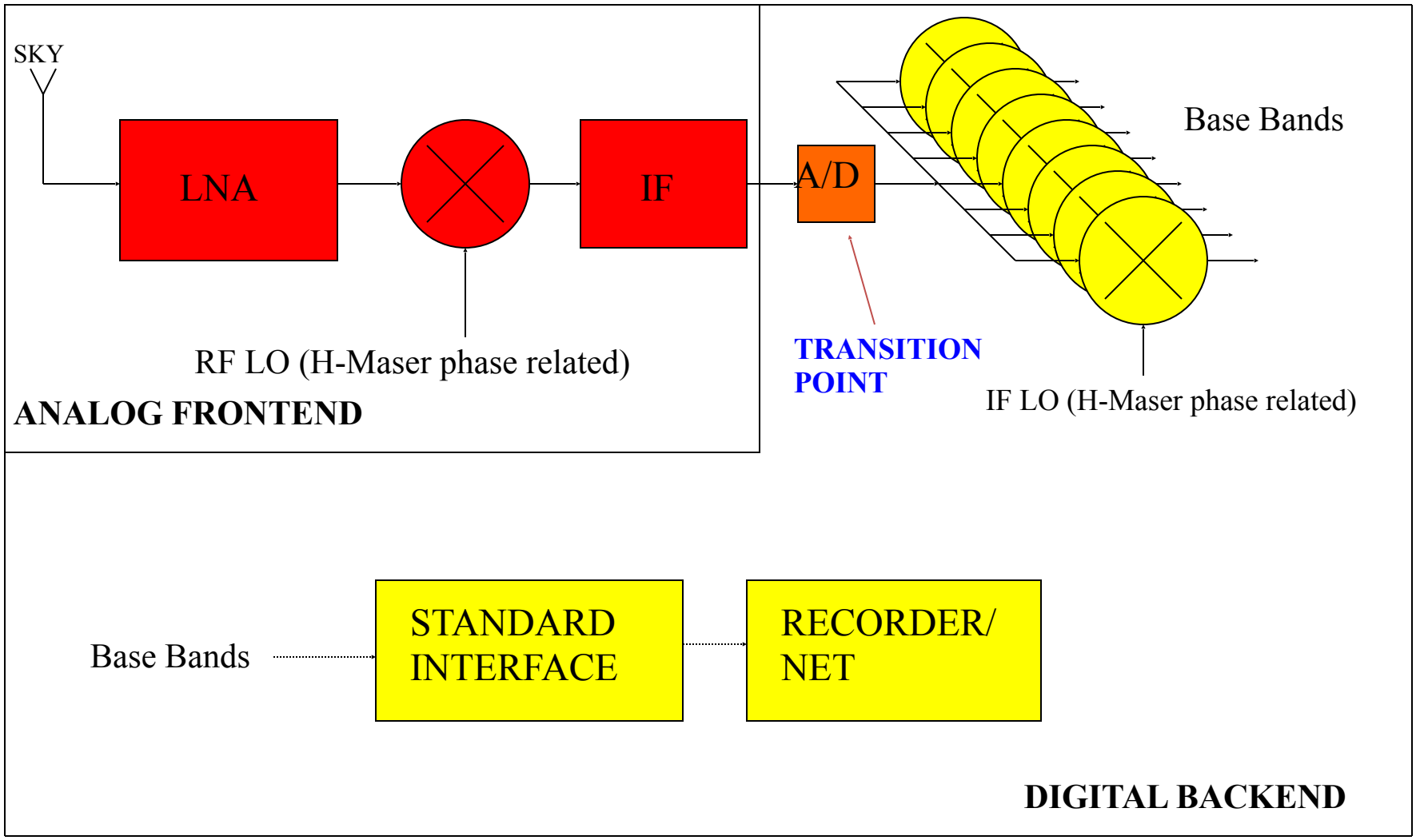
Front- and Back-End Multichannel Chain



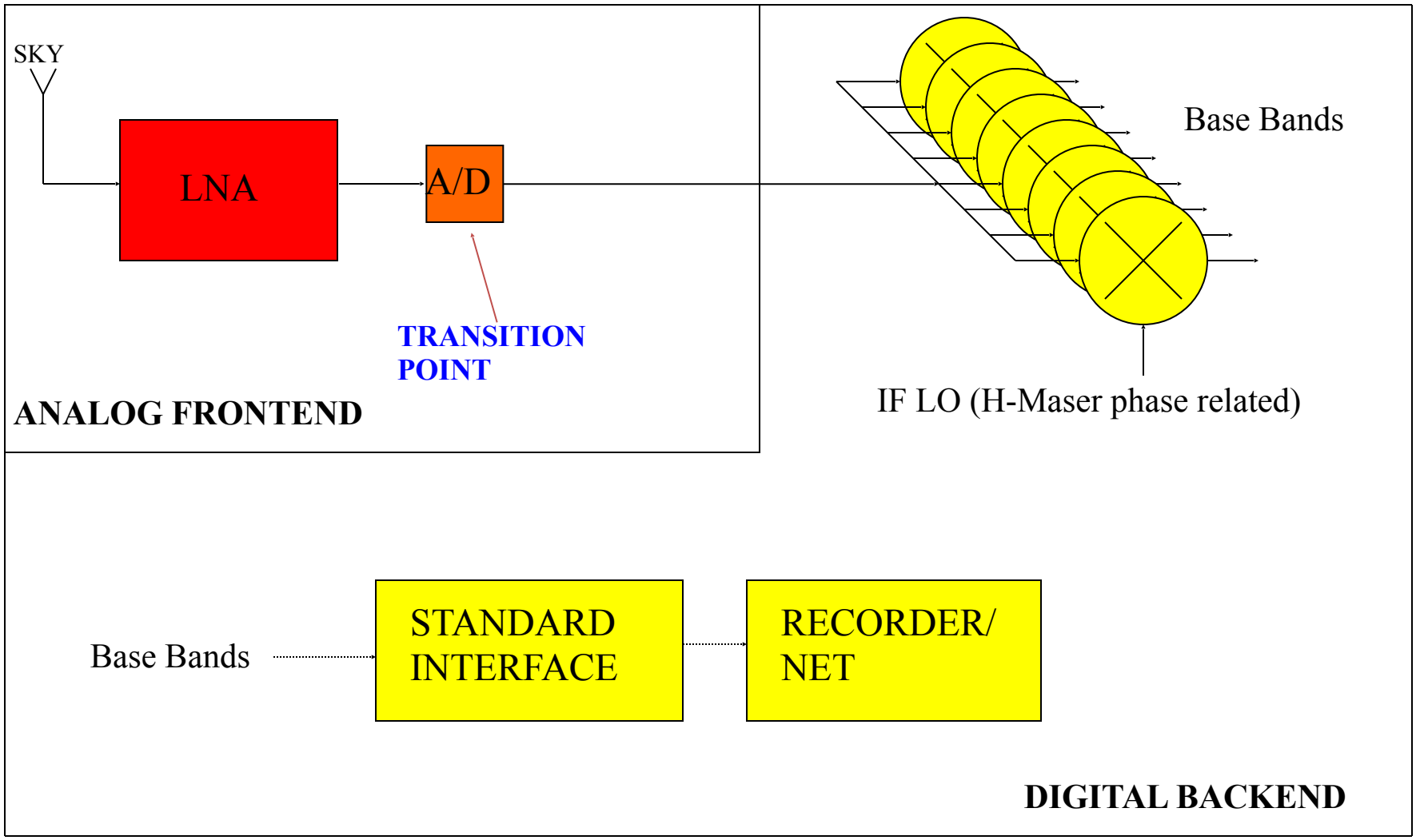
Front- and Back-End Multichannel Chain



Advanced Front- and Backend Chain



Advanced Front- and Backend Chain



Requirements ‘around’ the backend area

- Demand for an always wider bandwidth: receivers, data transport and correlators play their role, but backend should not be the bottle-neck
- New fast and powerful technologies are every day available
- New connectivity through a fast network is every day increasing
- Improvement of the phase stability in the entire signal path
- Obsolescence and difficulties in the analogue systems maintenance
- New radiotelescopes need new equipment
- More flexibility in number of bands and/or polarization
- More reliability

The need for a fully digital VLBI backend

- ‘Digital Radio’ technology become familiar within new telecommunication developments requiring frequency conversion
- Digital technology ready for the VLBI needed performance
- A new generation of stations (without any VLBI terminal) could also greatly benefit from new developments

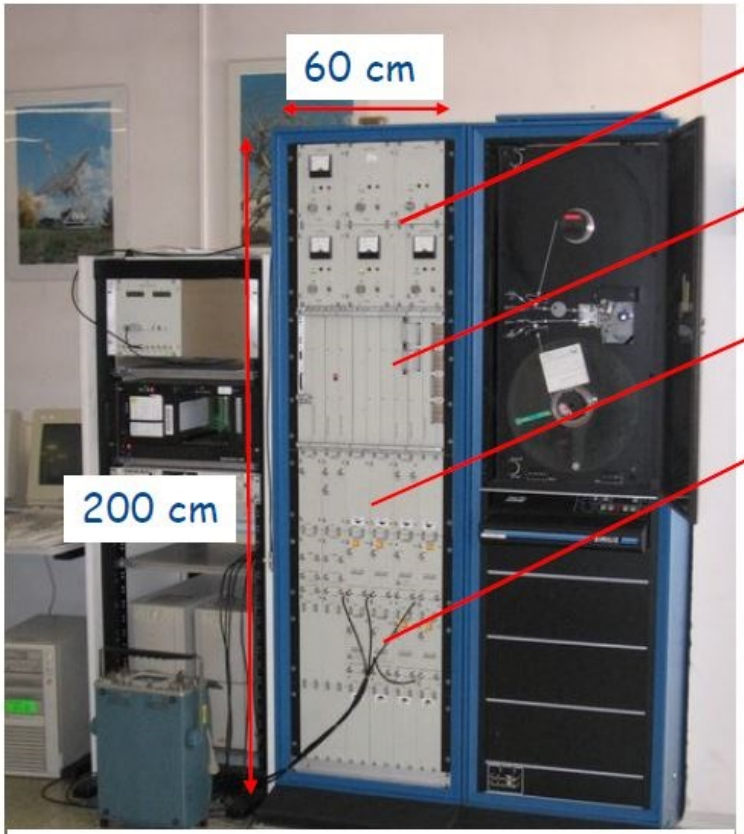
Why Digital?

- Digital is completely deterministic
- Precise and predictable modelling/performance
- Amplitude/Phase characteristics stable as sampling clock
- Wider, flatter pass-band, well matched between systems
- No dispersion and group delay distortion across the pass-band

Why more Digital?

- Much more compact implementation
- One hardware platform for many architectures and functions
- Cost effective for high performance multi-channel systems
- Process numerical with all the related implications
- RFI Mitigation can be greatly simplified

1980's vs 2000's



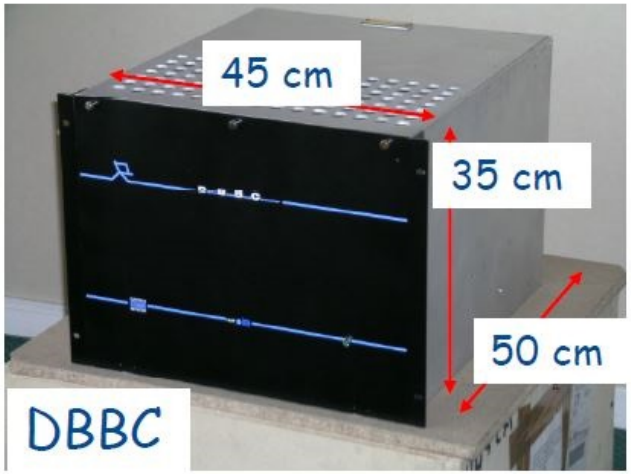
power supply

formatter

IF distributor

bbc

Analogue VLBA terminal & tape recorder.



DBBC

How to take this into consideration?

A general worldwide trend is to use more digital and less analog for predictability, repeatability, precision, etc.
This means to try and perform the

conversion from

ANALOG to DIGITAL

anticipated in the processing time as much as possible

and to use

DIGITAL SIGNAL PROCESS

General Functionality

Digital Backend Schematic Block

- Analogue to Digital Domain Conversion
- Digital Base Band Forming
- Output Streaming

General Functionality

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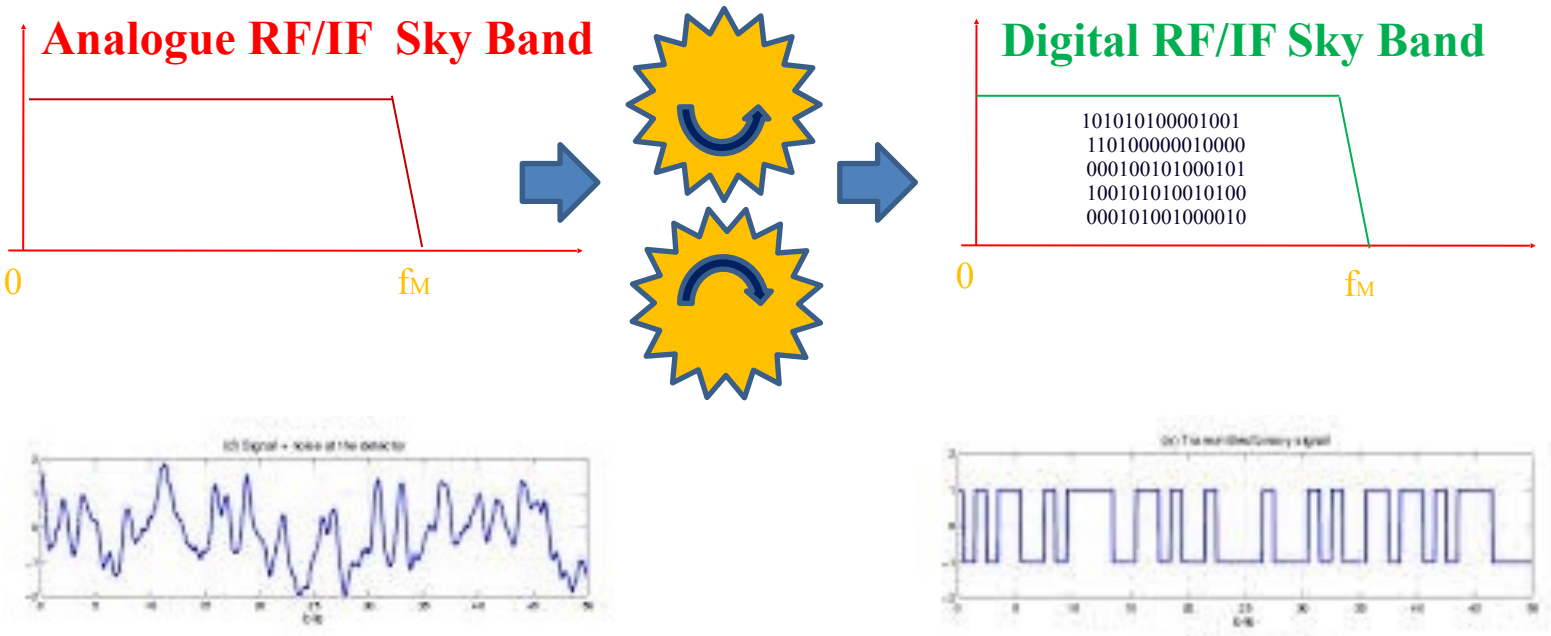
Analogue to Digital Domain Conversion

$$f_s = \frac{1}{\Delta t} \quad f_s > 2f_M$$



Processes involved in the analogue to digital domain conversion

- Sampling
- Nyquist criteria
- Aliasing
- Representation

Sampling

Sampling is the process to collect a sample of a signal, normally at a regular rate, with the aim to create an time ordered sequence of quantities to be used in a subsequent process. In our case we normally sample voltage values as coming from the receiver placed in the radiotelescope.

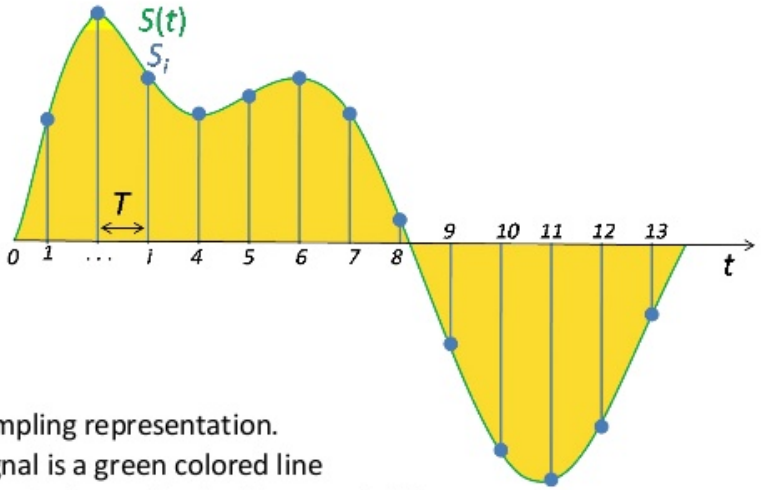
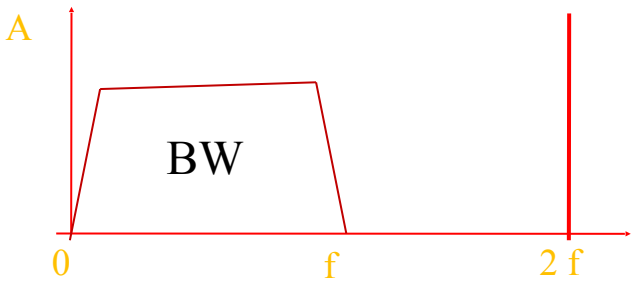


Figure 0: Signal sampling representation.
The continuous signal is a green colored line
Discrete samples are indicated by the blue vertical lines.

Nyquist Rate

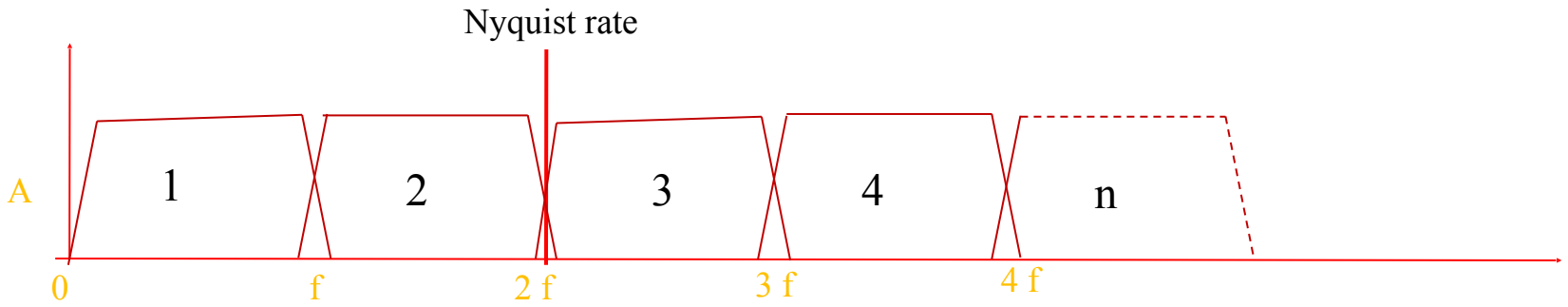


With a band limited signal BW (power spectrum only in a finite frequency band) no information is lost in the sampling process if its rate is greater or equal to 2 BW => Nyquist rate

Sampling rate is lower that the Nyquist rate => **under**sampling

Sampling rate is higher that the Nyquist rate => **over**sampling

Nyquist zones



- Providing that the Nyquist criterium is respected (Nyquist rate >= 2 BW) the frequency spectrum can be divided in zones, where each zone, at any frequency even higher than the Nyquist rate, can be represented by a sampling process without any loss of information. Limitation in such a concept is the real bandwidth of the hardware devices in the high boundary.

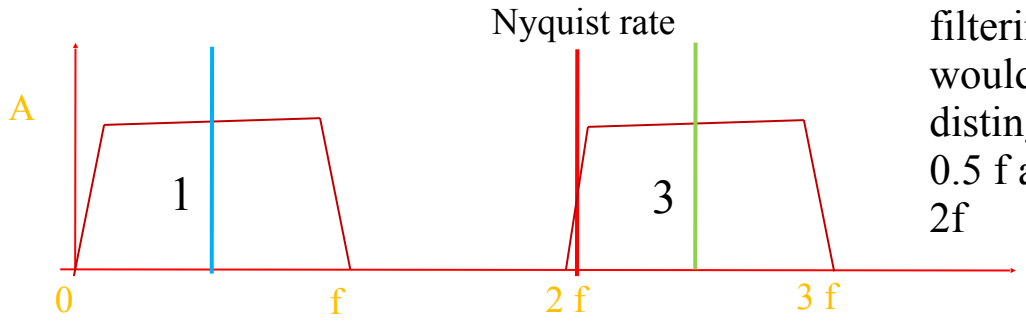
- A single sampled Nyquist zone is actually translated in base band (Nyquist zone 1), with only even zones reversed in frequency, being the odd ones unreversed

- The sampling process can be seen like a frequency conversion process

Aliasing

Aliasing is the misidentification of a signal frequency, introducing ambiguity, distortion, error in the analogue to digital conversion

Analog signals are usually band-pass filtered to remove most or all of the components not respecting the Nyquist criteria in order to avoid aliasing



For example: sampling without filtering Nyquist zone 1 from 3 would bring to not be able to distinguish between two tones at 0.5 f and 2.5 f, with Nyquist rate 2f

Digitization - Numerical Representation

- The digitization process is the representation of a samples by generating their numerical discrete value representing the required quantity to be processed in the digital domain.

- Samples are rounded to a fixed set of numbers (normally integers) and such process is known as quantization.

- The numerical representation of the sampled signal requires careful choices to take into account the required dynamical range.

Number of bit for representing the samples

- Digital electronics operates in binary numerical representation, then a sequence of words of n-bit is the adopted representation

- How many different values can represent a n-bit sample?

$$\mathbf{2^n}$$

1-bit can represent for example the sign (+/-) of a signal

2-bit can be able to represent 4 levels, so if positive or negative, if higher or lower than a certain positive (and negative) value

and so on …..

8-bit can distinguish between 256 different levels

An infinite number of bit is the analogue representation of the signal

How the number of bit representation affect the sensitivity

A trade-off between the number of levels to represent samples and output data rate from the backend to the recorder is to be taken into account in order to optimize the sensitivity and the effective capability to store and correlate astronomical data

An efficiency factor affecting the sensitivity is expressed by the ratio between quantized and unquantized data:

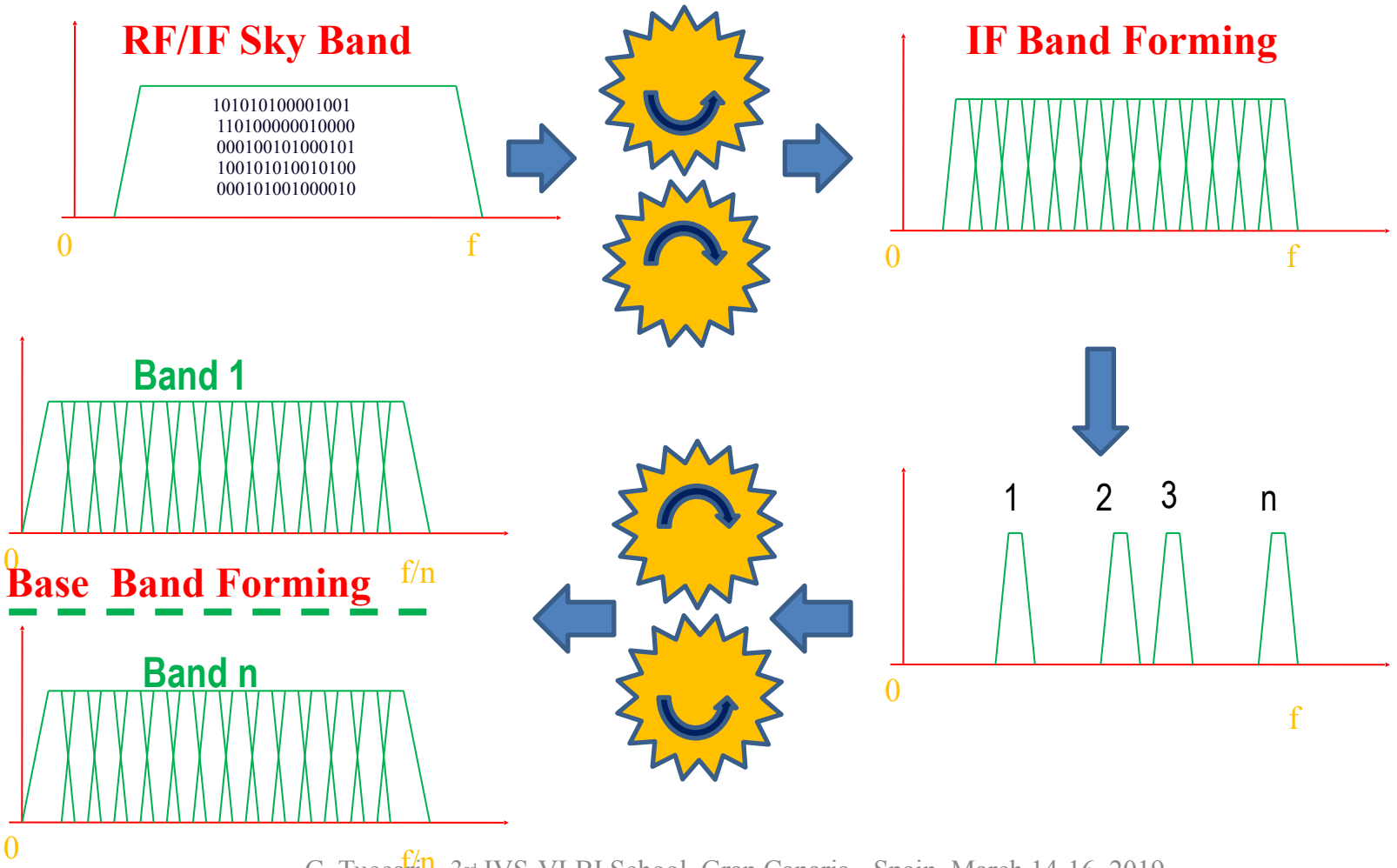
2 levels (1-bit) => 0,64
3 levels (2-bit) => 0.81
4 levels (2-bit) => 0.88 mostly adopted

General Functionality

Digital Backend Schematic Block

- Analogue to Digital Domain Conversion
- Digital Base Band Forming
- Output Streaming

Digital Base Band Forming



Processes involved the base band forming

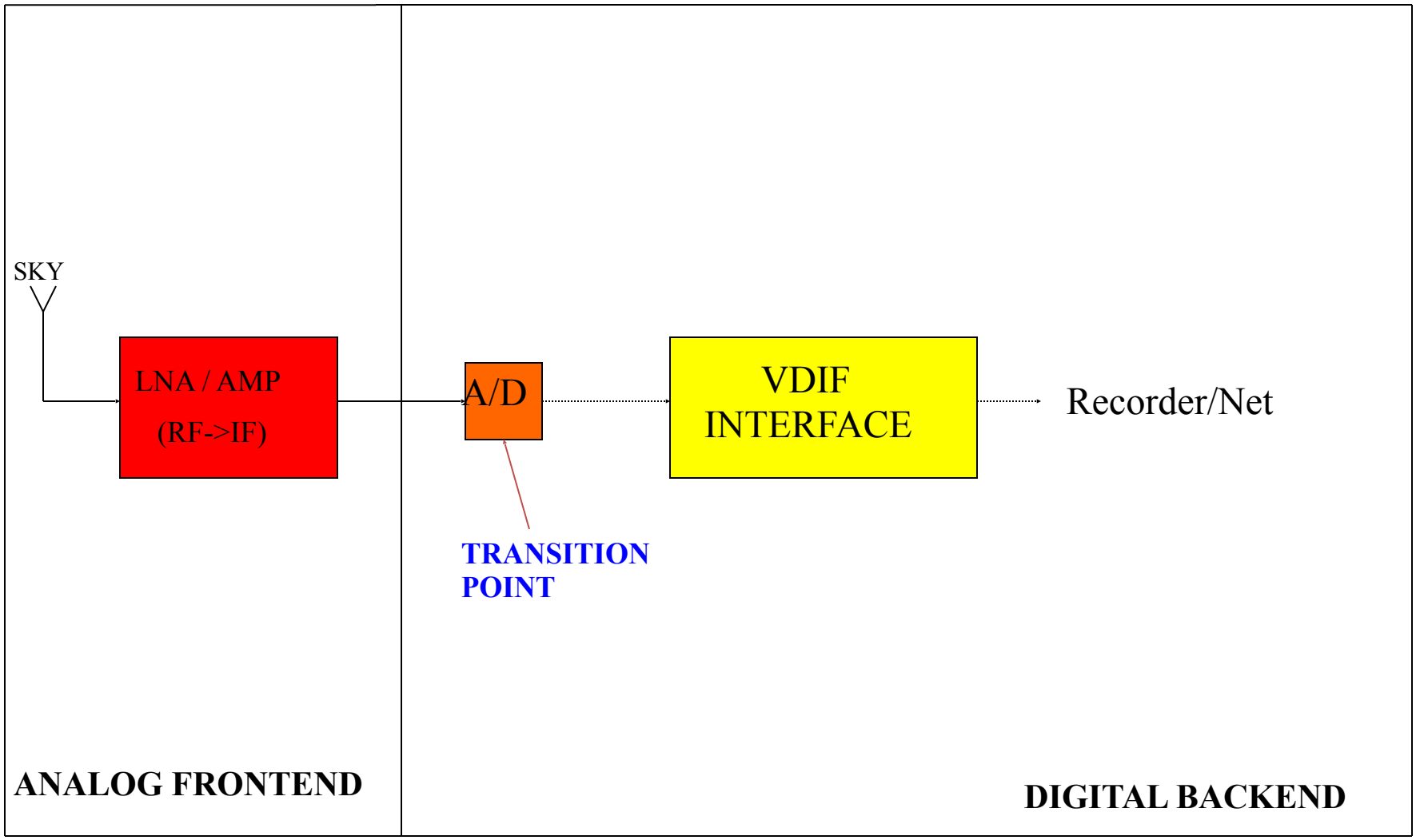
- Number of channels and their bandwidth
- Time tagging
- Output representation
- Ancillary functionalities

Different modes for converting

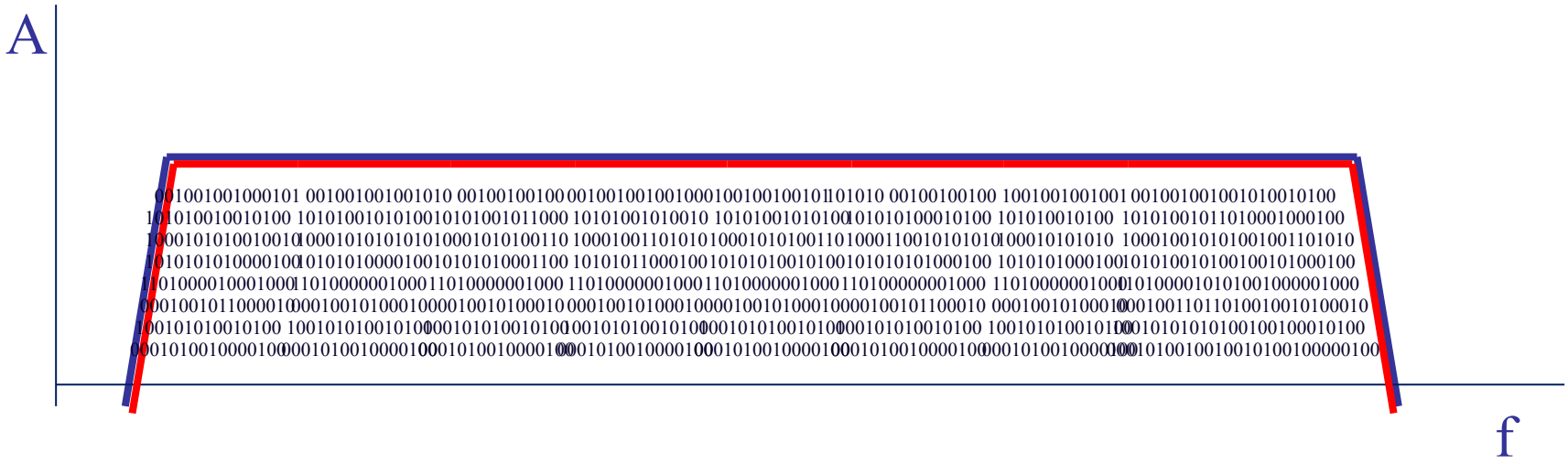
- A main distinction in the backend data process is the number and the bandwidth of the slots of bands to be used for correlation. Those parameters depend mainly on the type of scientific observation and on the actual capability (bandwidth/data rate) of the entire acquisiton chain.

- Different modes have been defined and used in the course of the years and a VLBI standard was agreed among the worldwide radiotelescopes working in network

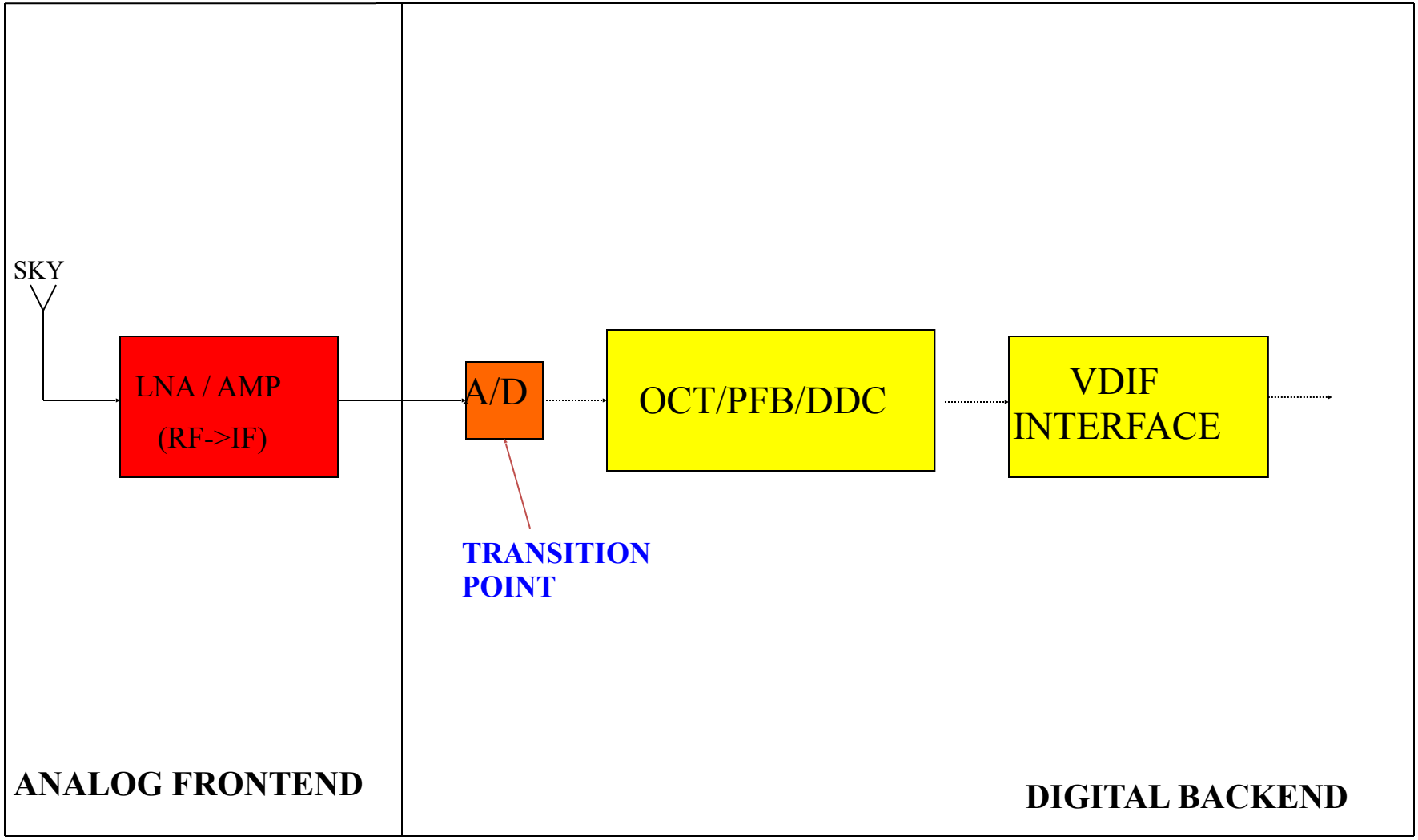
Direct Sampling Conversion



DSC – Direct Sampling Conversion

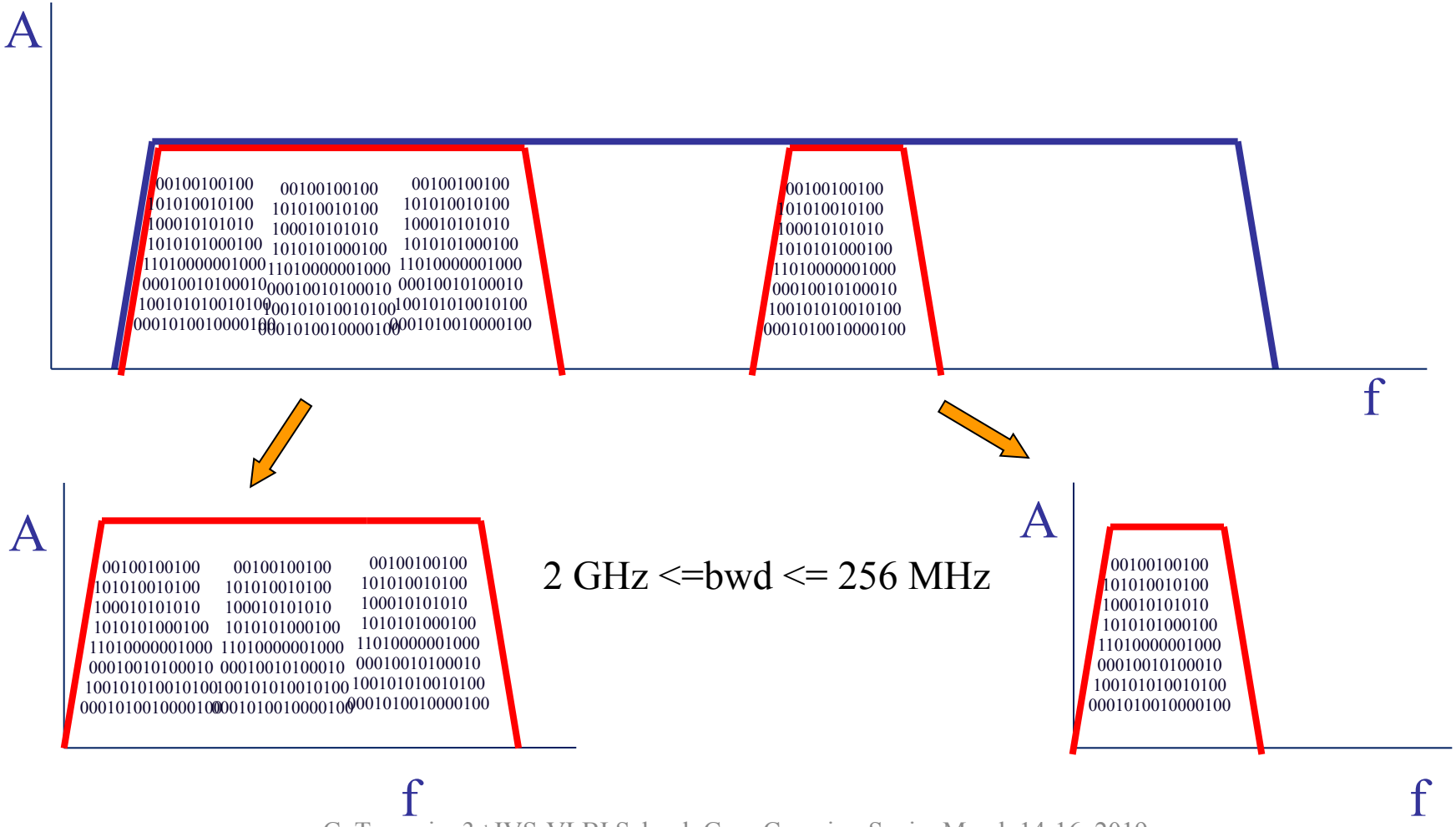


OCT/PFB/DDC – Base Band Conversion

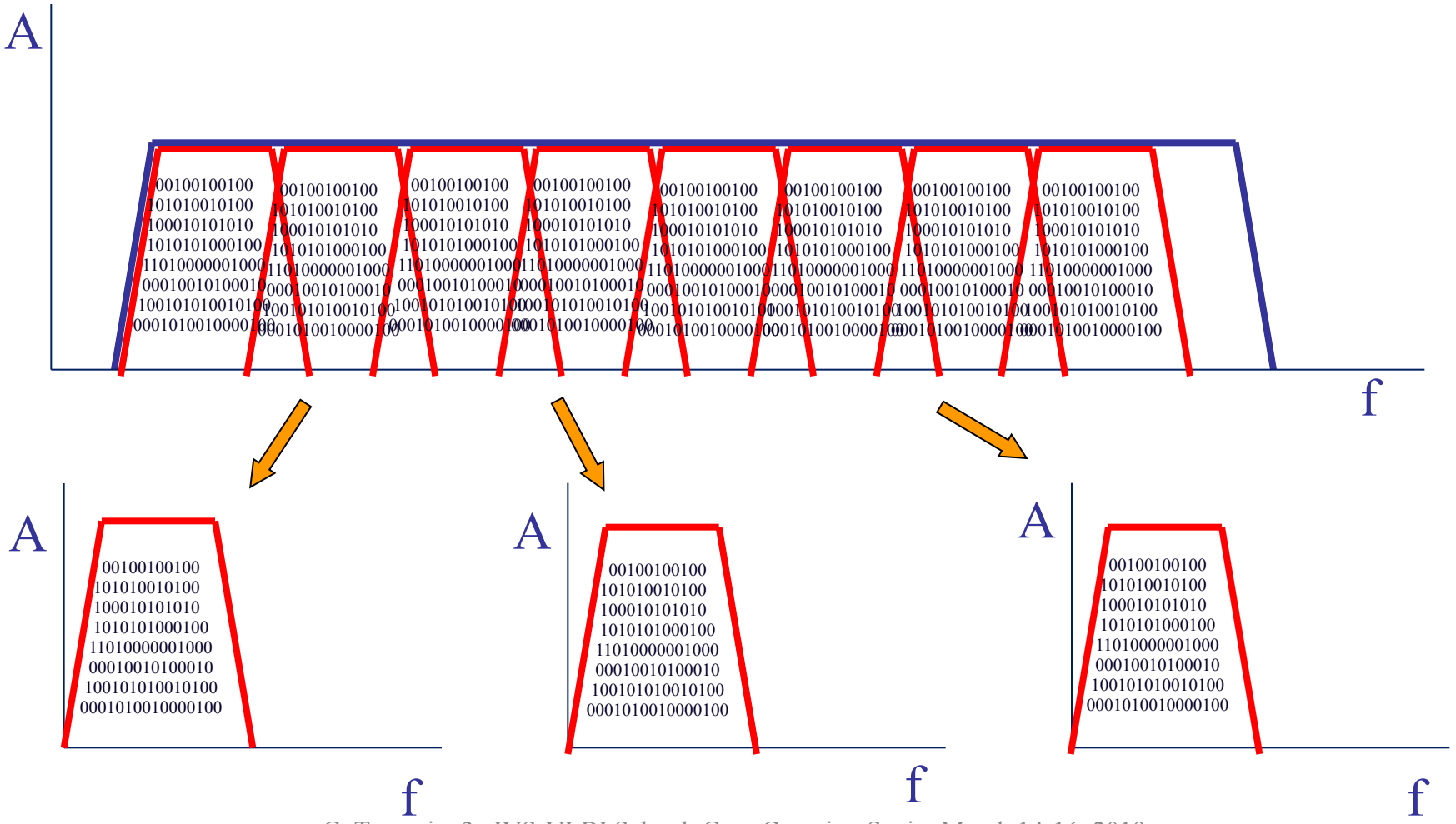


OCT - Flexible Broad Band Channel Formation

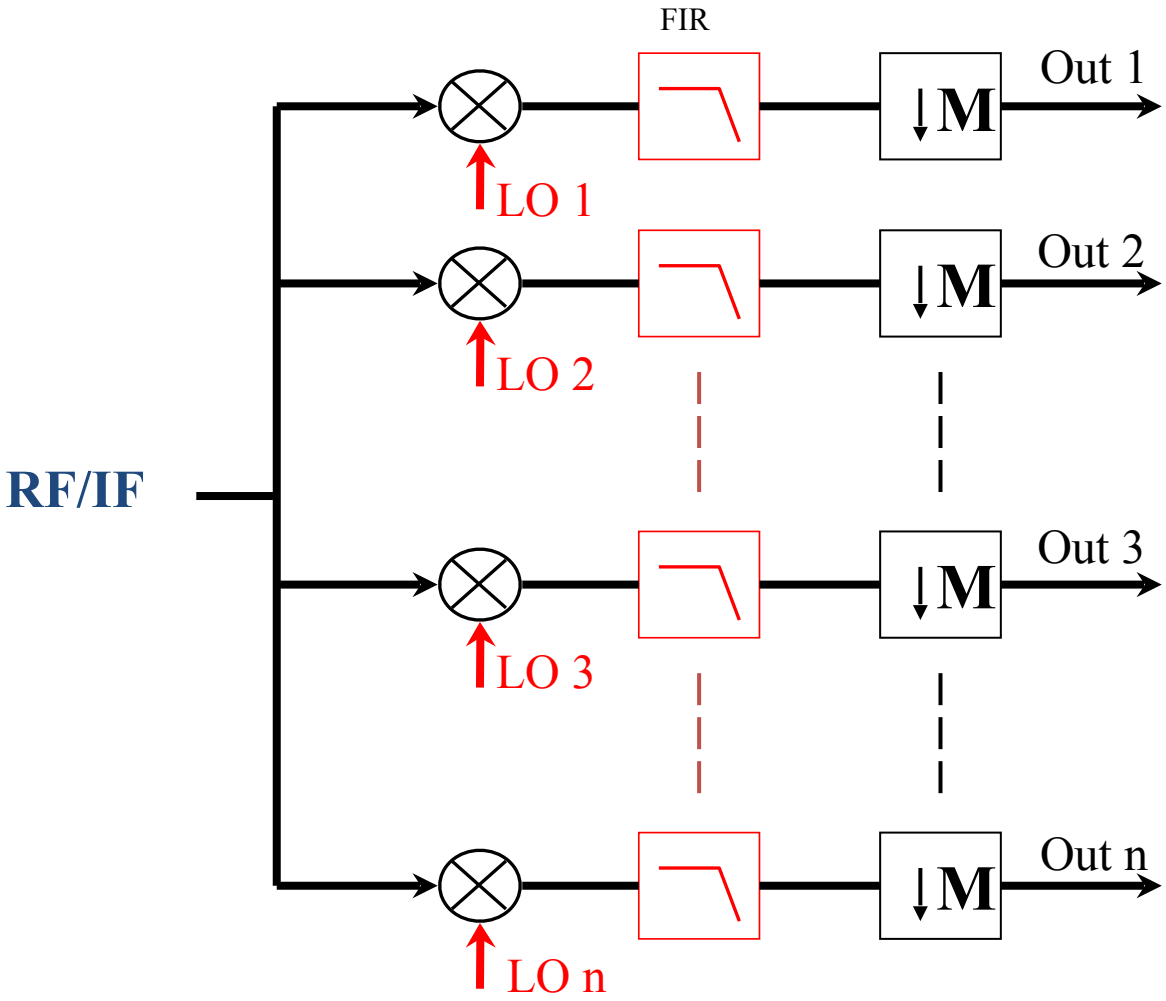
(mainly used 2 GHz (EHT), 1 GHz (Kashima), 256 MHz (EAVN))



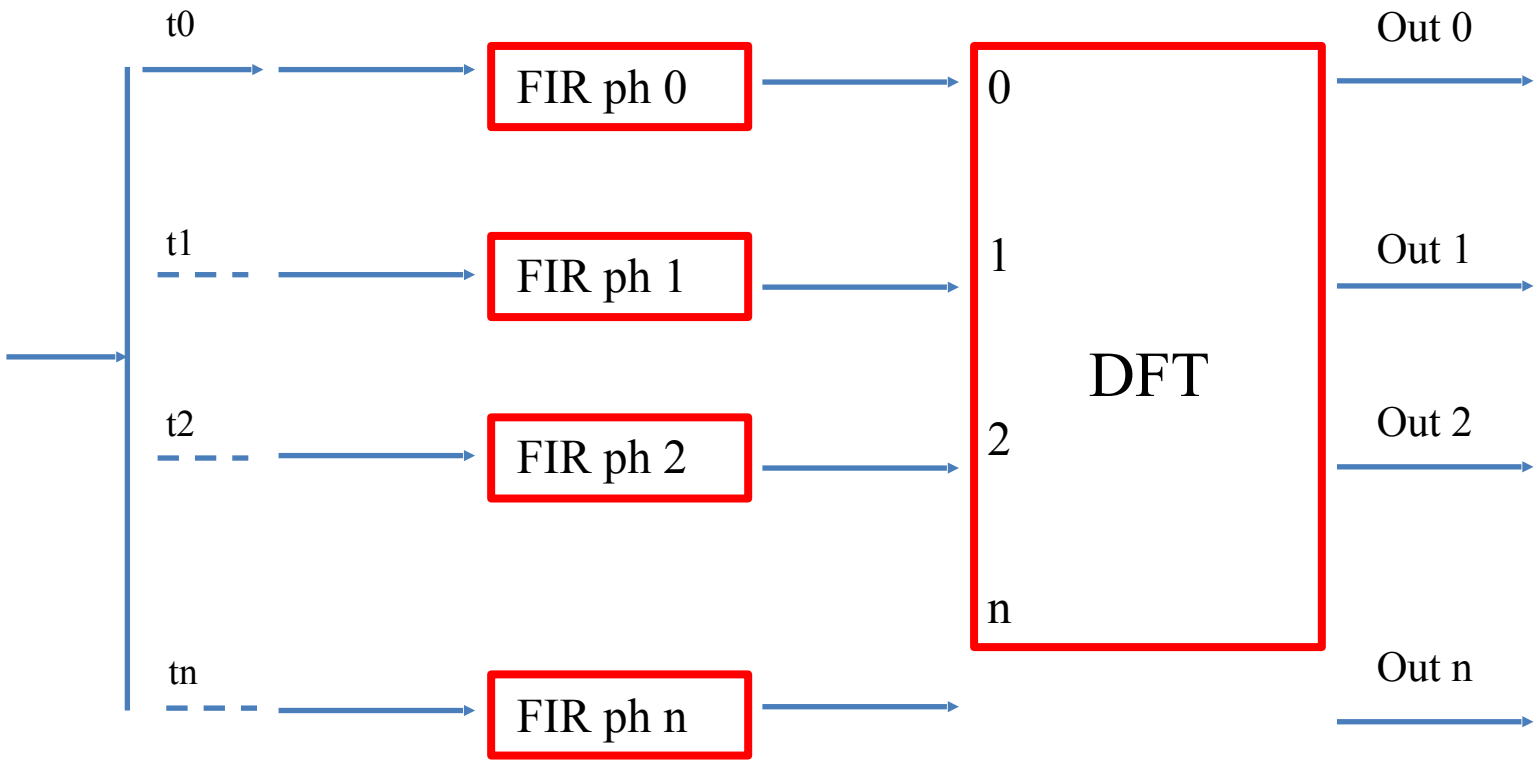
PFB - Multi Equispaced Channel Conversion to Base Band
Polyphase Filter Bank (mainly used in VGOS 32MHz)



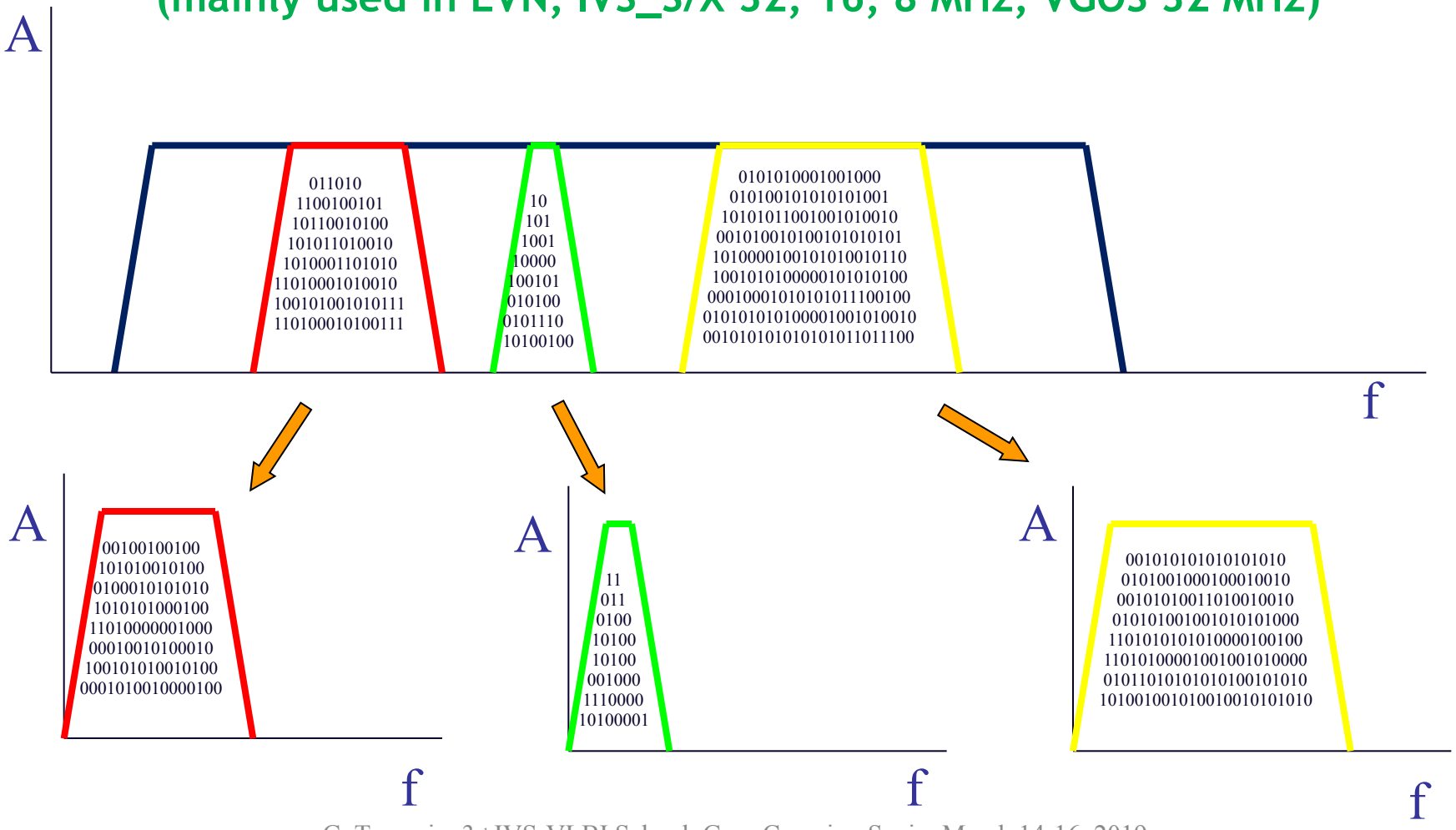
PFB – Polyphase Filter Bank Conversion to Base Band



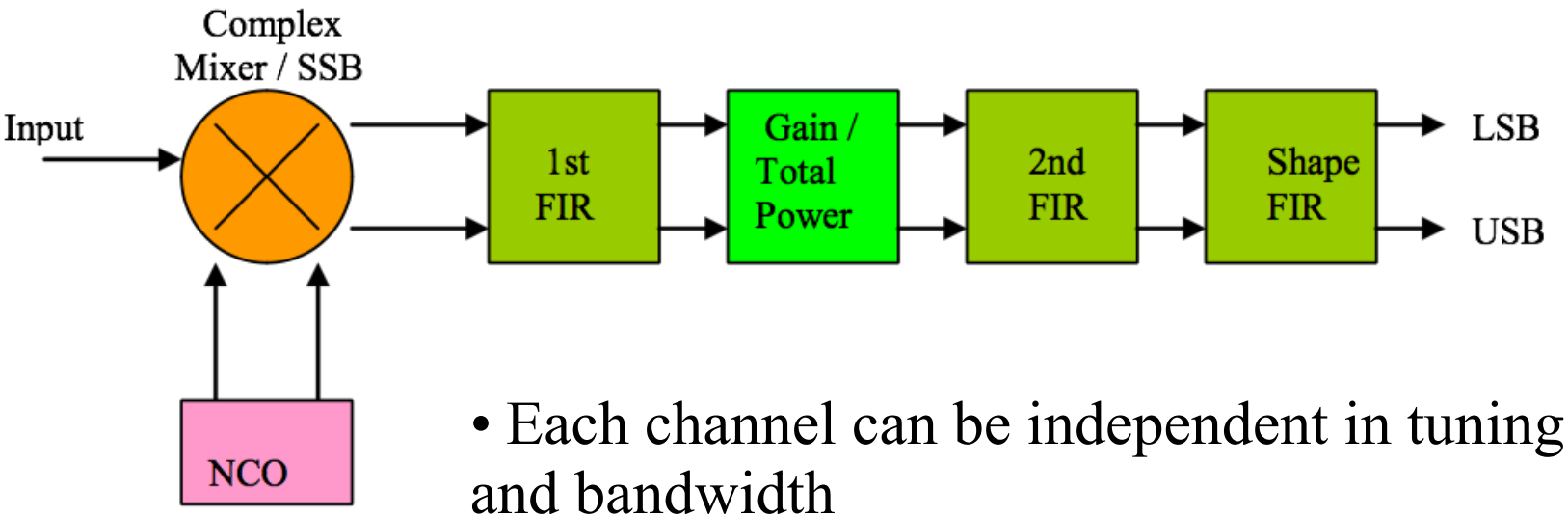
PFB – Poly Phase Filter Bank Solution



DDC - Digital Down Conversion
to Base Band of Independent Channels
(mainly used in EVN, IVS_S/X 32, 16, 8 MHz, VGOS 32 MHz)



DDC - Digital SSB Schematic View



- Each channel can be independent in tuning and bandwidth
- More channels possible

Digital Backend Systems Available

- American RDBE, RDBE2
- Chinese CDAS
- European DBBC2, DBBC2010, DBBC3
- Japanese VERA, GALA-V
- Russian BRAS

DBBC Example

DBBC Back-ends evolution

DBBC1 2004 - 2008

in: 4 x IF-512MHz

out: **DDC** 16 x bbc (1-2-4-8-16MHz)@32MHz

0.512/1.024 Gbps

DBBC2 2007 – today

in: 4 x IF-512/1024MHz

out: **DDC** 16 x bbc (1-2-4-8-16-32MHz)@32/64MHz

PFB 4 x 16 x (32-64 MHz)@64/128MHz

4.096/8.192 Gbps

DBBC2010 2009 – today

in: 8 x IF – 512/1024MHz

out: **PFB** / **DSC** **16.384/32.768 Gbps**

DBBC Back-ends evolution

DBBC3L (-2L2L) 2014 – today **EVN32Gbps / EHT**

in: 2 x IF-4096 / 4 x IF-2048 / 8 x IF-1024

out: **DDC** 8-16-32-64-128 MHz

PFB (and mixed) 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

16/32 Gbps

DBBC3L (-4L4H) 2014 – today **VGOS half-compliant**

in: 4 x IF-4096 / 8 x IF-2048 / 16 x IF-1024

out: **DDC** 8-16-32-64-128 MHz

PFB (and mixed) 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

16/32/64 Gbps

DBBC Back-ends evolution

DBBC3L (-8L8H) 2014 - today **VGOS full-compliant**

in: 8 x IF-4096 / 16 x IF-2048 / 32 x IF-1024 MHz

out: **DDC** 1-2-4-8-16-32-64-128-256 MHz

PFB **PFB** (and mixed) 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

16/32/64/128 Gbps

DBBC3H (-2H2H/-4H4H) end 2017 **VGOS full-compliant**

in: 2 x IF-14336 MHz

out: **DDC** 1-2-4-8-16-32-64-128-256-512-1024 MHz

PFB (and mixed) 32-64-128-256-512-256-512-1024 MHz

DSC 1024-2048-4096-8192-14336 MHz

16/32/64/128/229 Gbps

DBBC1 (2004) and DBBC2 (2007) General Features

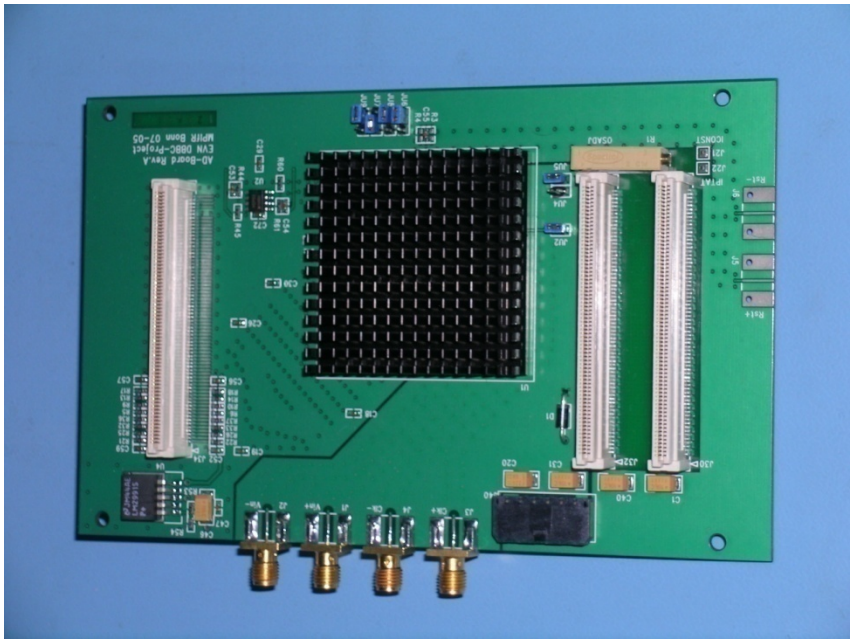
- DBBC1: Four IF Input in the range 10-512 or 512-1024 MHz
- DBBC2: Four IF Input in the range 10-512, 512-1024, 1024-1536, 1536-2048, 2048-2560, 2560-3072, 0-1024 MHz, L band
- 1024 or 2048 MHz fixed frequency sampling clock
- DBBC1: Channel bandwidth ranging between 1MHz to 16 MHz
- DBBC2: Channel bandwidth ranging between 1MHz to 32 MHz
- Tuning step for VLBI 10 KHz
- Multiple architecture using fully re-configurable FPGA
- Modular realization for possible cascaded processing
- Field System support

DBBC1/2 General Features (cont.)

- Data out as single or double VSI interface
- Total power measurement capability
- Continuous Tsys measurement capability
- Digital to analog converter monitor output
- Digital AGC
- Optional 10 gigabit data shifter (see later)

ADB1

Analog to Digital Converter



Analog input: 0 - 2.2 GHz

Max Sampling clock single board: 1.5 GHz

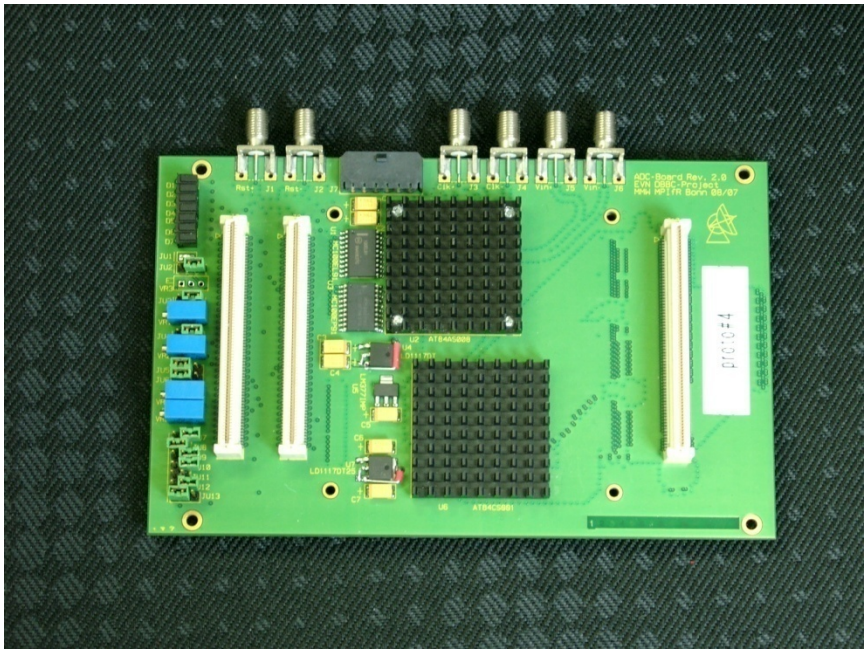
Max Istantaneous Bandwidth in Real Mode: 750 MHz

Max Istantaneous Bandwidth in Complex Mode: 1.5 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR

ADB2

Analog to Digital Converter



Analog input: 0 – 3.5 GHz

Max Sampling clock single board: 2.2 GHz

Max Istantaneous Bandwidth in Real Mode: 1.1 GHz

Max Istantaneous Bandwidth in Complex Mode: 2.2 GHz

Output Data: 2 x 8-bit @ ¼ SClk DDR
4 x 8-bit @ 1/8 SClk DDR

Piggy-back module support for 10-bit output and connection with FiLa10G board.

CORE2

Basic processing unit

Input Rate:
(4 IFs x 2 bus x 8 bit x SClk/4 DDR) b/s
(2 IFs x 4 bus x 8 bit x SClk/8 DDR) b/s
More…

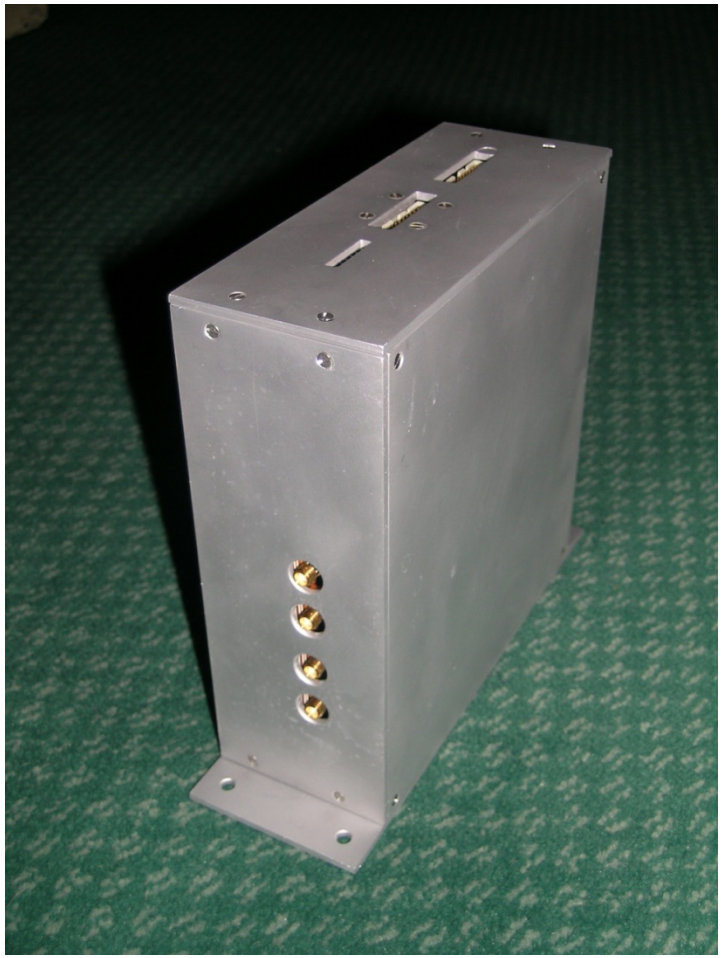
Typical Output Rate:
(64 ch x 32-64-128-256) Mb/s

Programmable architecture

Es. Digital Down Converter:
1 CoreBoard2 = 4 BBC

Max Input/Output Data Rate 32.768 Gbps

ConditioningModule



Pre-AD Conversion Analog Signal Conditioning

Pre-AD Conversion Band Definition

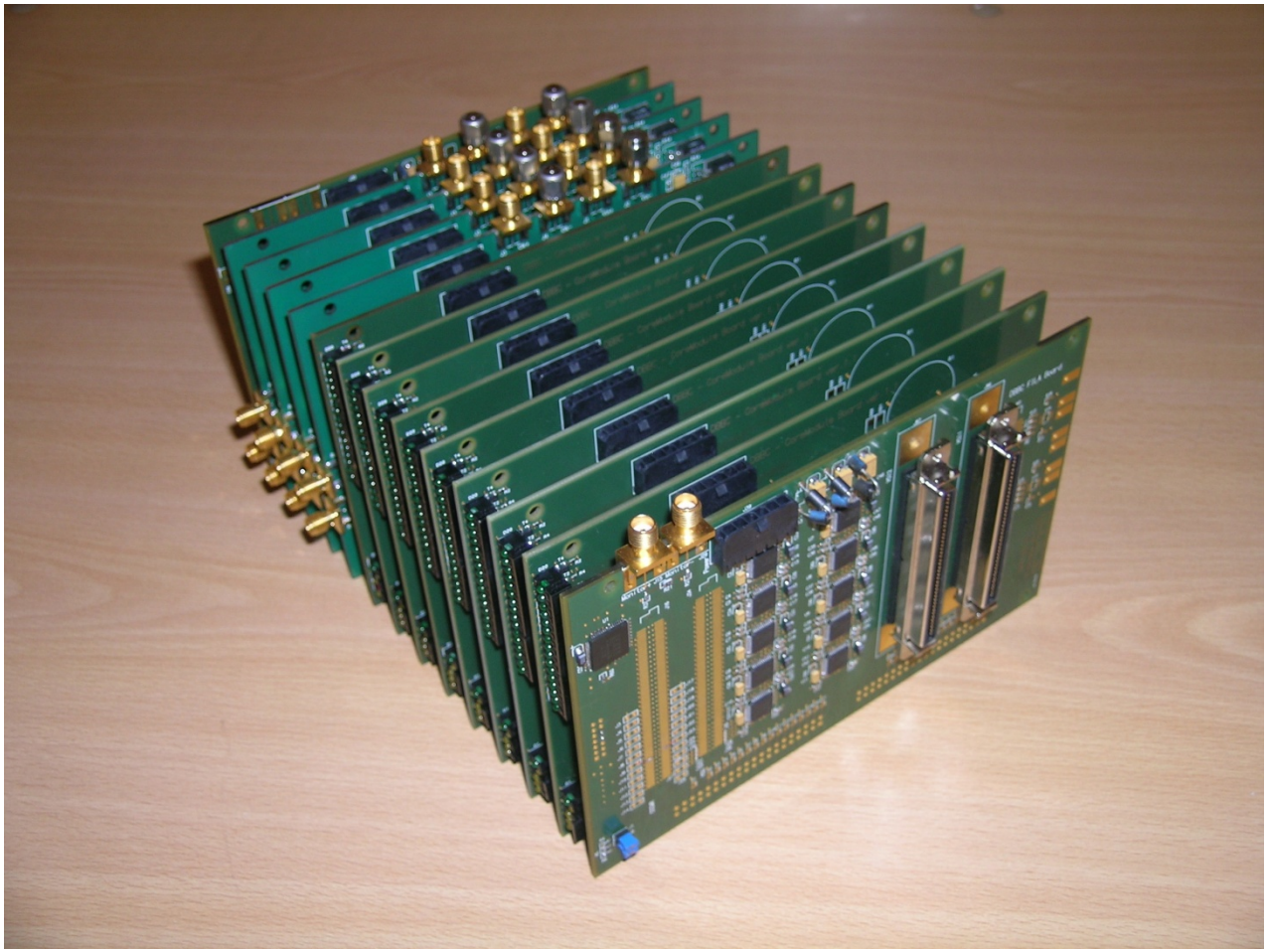
4 IFs Selectable Input

Total power measurement

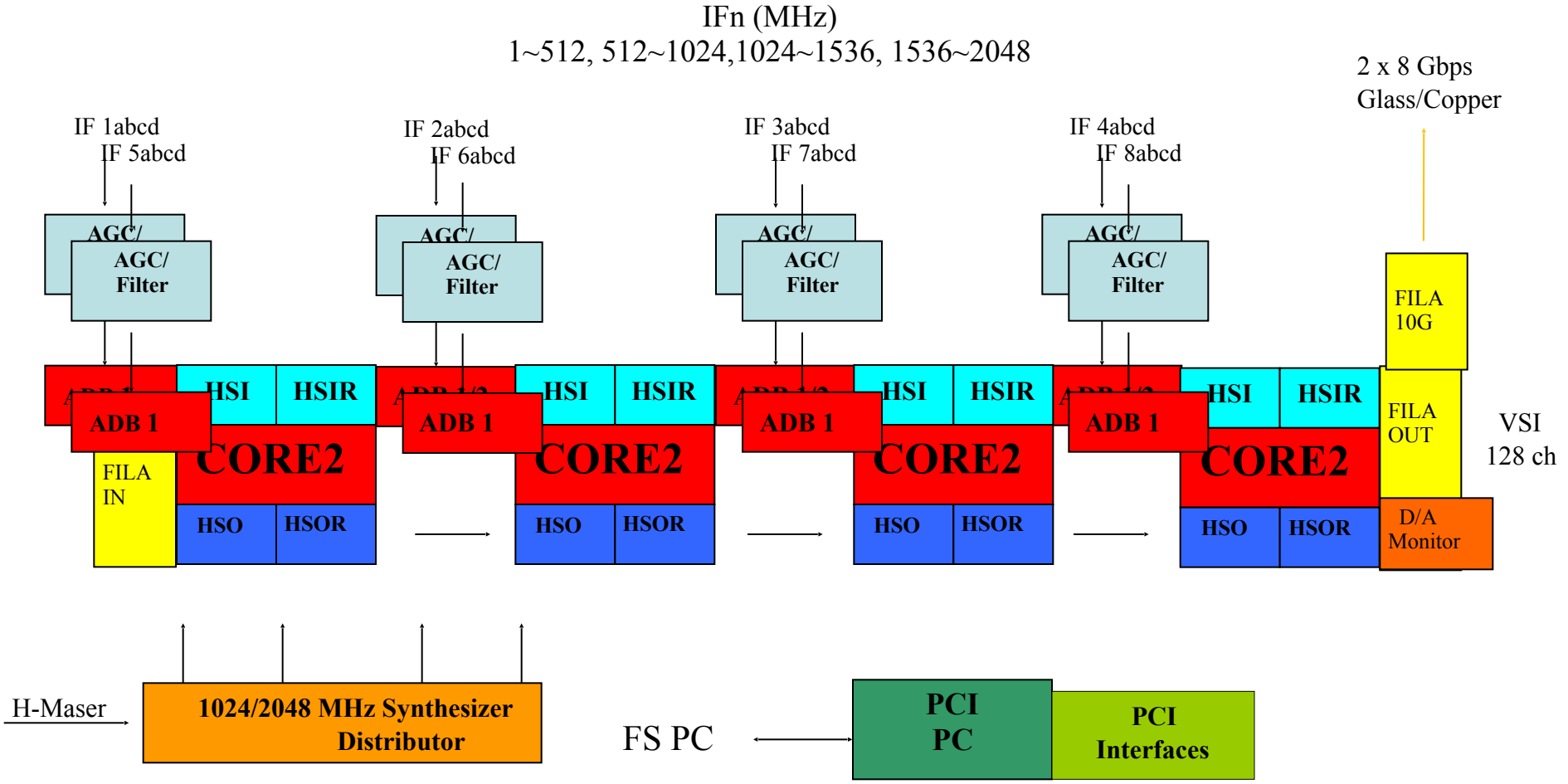
RF Gain Control

Amplitute equalization

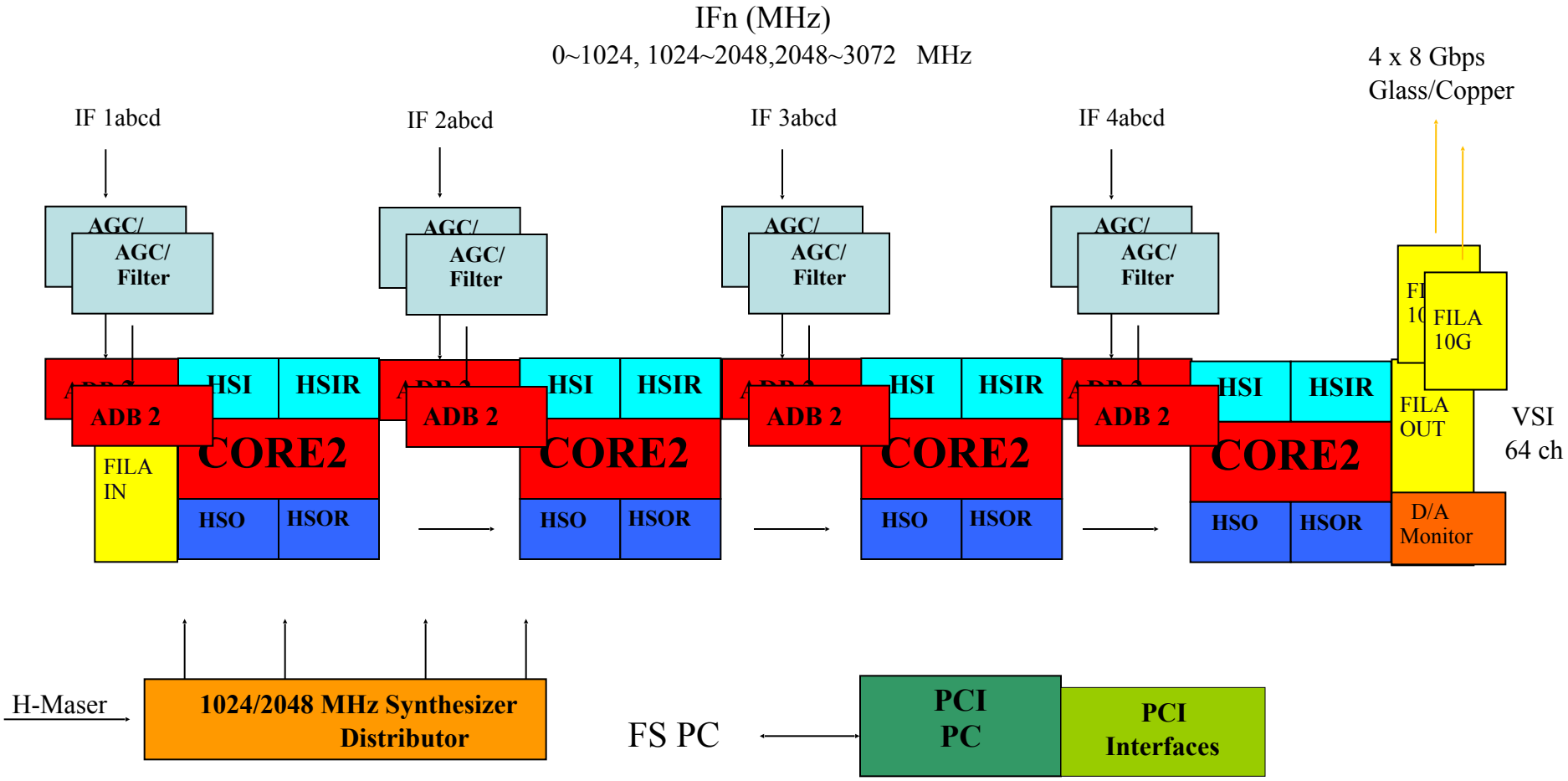
4 ADB1 + 8 CORE1 Stack



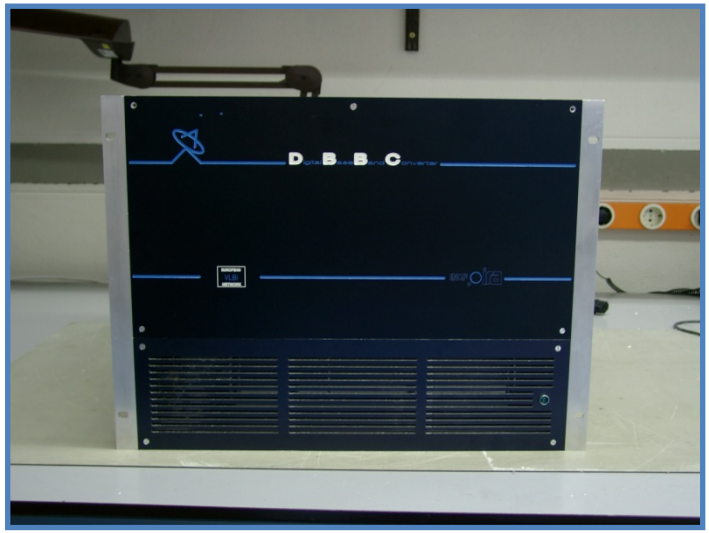
DBBC2010 Architecture A
8 IFs @ 512 MHz
Output data rate 16Gbps

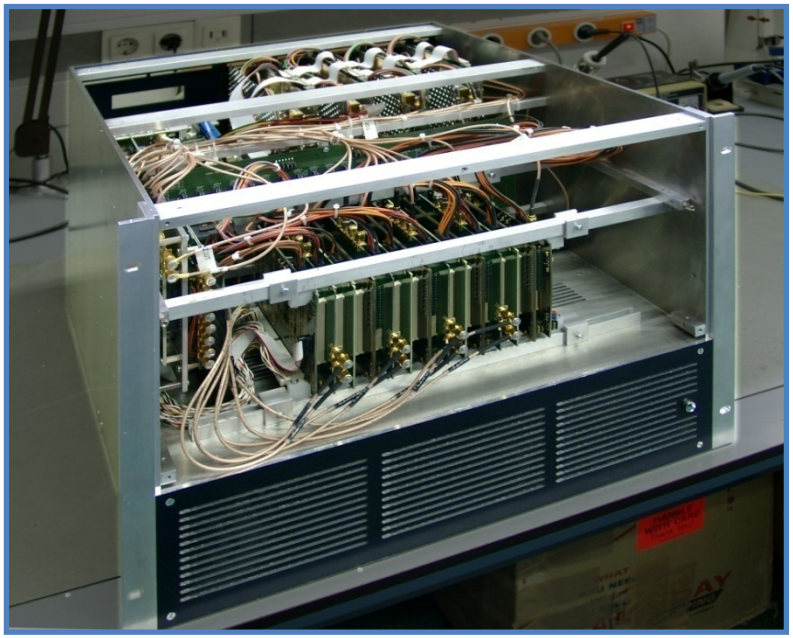


DBBC2010 Architecture B
8 IFs @ 1024 MHz
Output data rate 32Gbps



DBBC1/2 photos





Network Board

FILA10G

- FILA10G the interface between the DBBC (or any VSI device) to 10G network
- The board shfts interface for the MK5C or as direct connection to the network at 1–2–4–10–20 Gbps
- Can be used as standalone between VSI and network
- Can be used as standalone with ADB2
- MK5B and VDIF compliant (corner turner included)

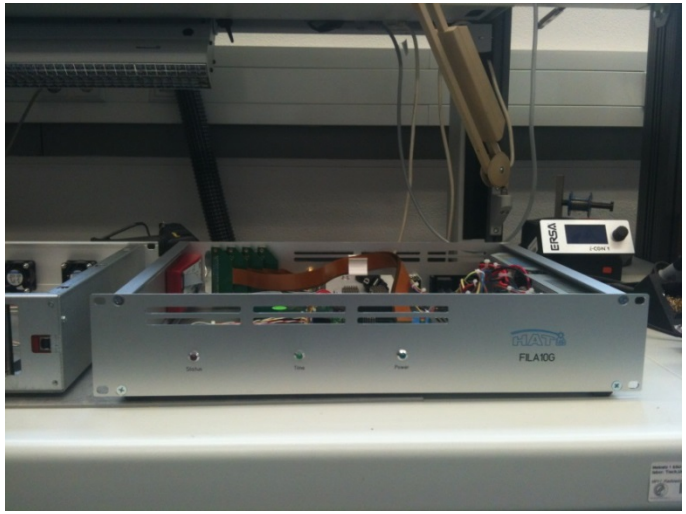
10GE Output Stream

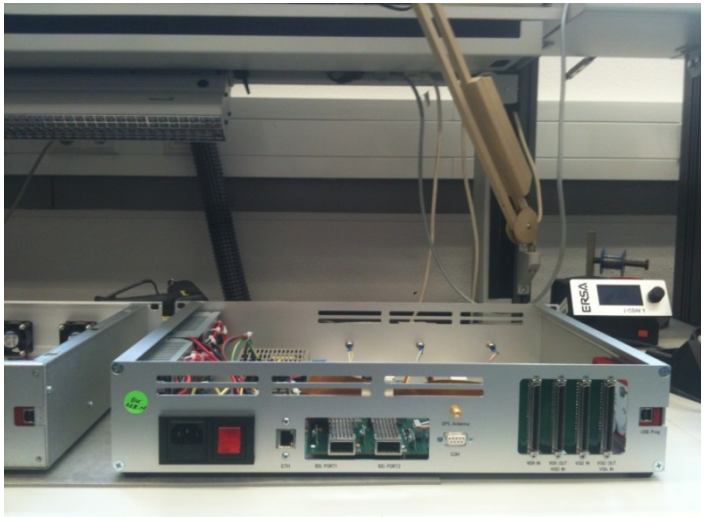
Output is a set of 10GE connections (optical or copper):

- MK5B
- VDIF - Multichannel single thread
- VDIF - Corner turned data with multiple threads carrying single band channels
- Multiple destination address for the multiple threads in the data streams
- Raw

FILA10G Shifts VLBI data on Internet – 16 Gbps
4 x VSI-H <> 2 x 10GE

- MK5B up to 4 Gbps
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads
- RAW (no headers)
- Threads eventually corner-turned
- The 10G Ethernet ports independent in destination address in VDIF-ST and MK5B
- Multi-thread mode support an independent block of destination addresses
- Decimation and bit-mask selectable





DBBC3 (2014)

- Development started for a new set of boards to increase maximum bandwidth and data rate
- Compatible with precedent versions (replacement of boards in the stack, or mixed operation)
- New CoMo: 6 GHz bwd
- New CaT: integrates Clock and Timing boards and allow interleaved operations
- New Core3

DBBC3L (2014) Radionet 3

General Performance

- Number of RF/IF in one system: **std. 2 (8 for VGOS)**
- Instantaneous bandwidth each sampler: **4 GHz**
- Sampling representation: **10 bit**
- Processing capability**: std. 24** (**max 96) TMACS** (multiplication-accumulation/s)
- Output: **VDIF 10GE/40GE packets, 32/64/128 Gbps**
- Observing Modes: **DDC/PFB/DSC**
- Compatibility with existing DBBC2 environment

DBBC3L is aiming at:

Astronomy

- **EVN wide-band VLBI backend**
- **EHT (Event Horizon Telescope)**

Geodesy

- **VGOS ultra-wide-band VLBI system**

DBBC3-L Architecture for EVN and EHT

GCoMo (GigaConditioningModule)

Additional element to adapt the receivers

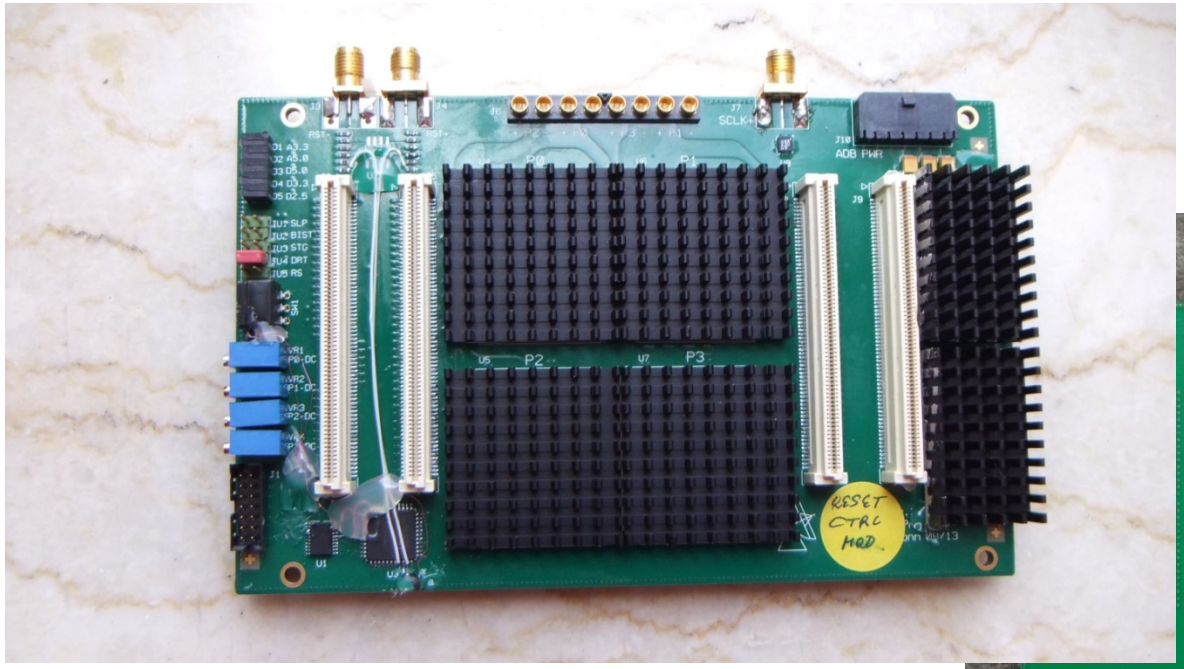
- Downconvert pre-filtered pieces of 4 GHz bandwidth
- Input range: up to 16 GHz
- Number of channels: 2 pre-filtered 4 GHz bands
- Total power detectors: 2 independent
- Power level control in agc and manual mode
- Compatibility with existing DBBC environment

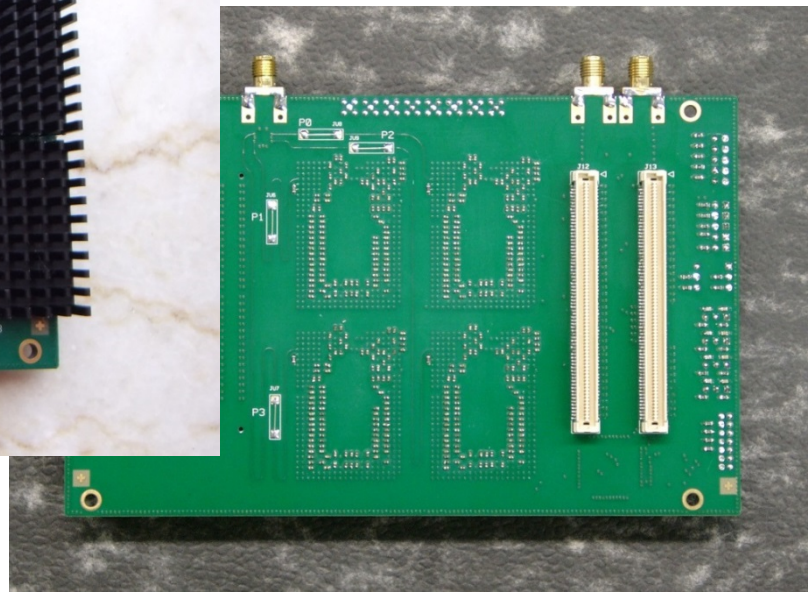
ADB3L - Sampler board

- 4 x 1 GHz samplers combined
- Number of IFs: **1 - 4**
- Equivalent Sample Rate: **2-4-8 GSps**
- Instantaneous bandwidth: **1-2-4 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC environment

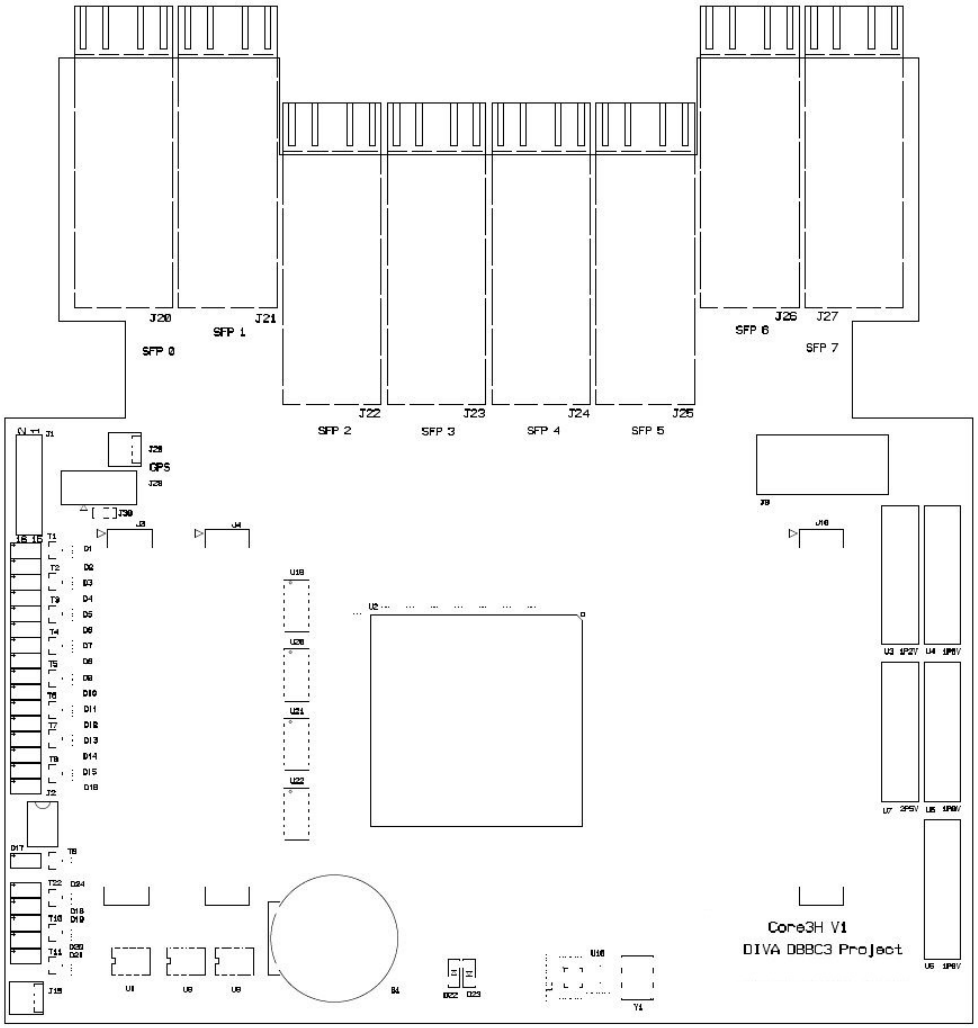
Status ADB3L

Prototype ready debugged, final revision under construction



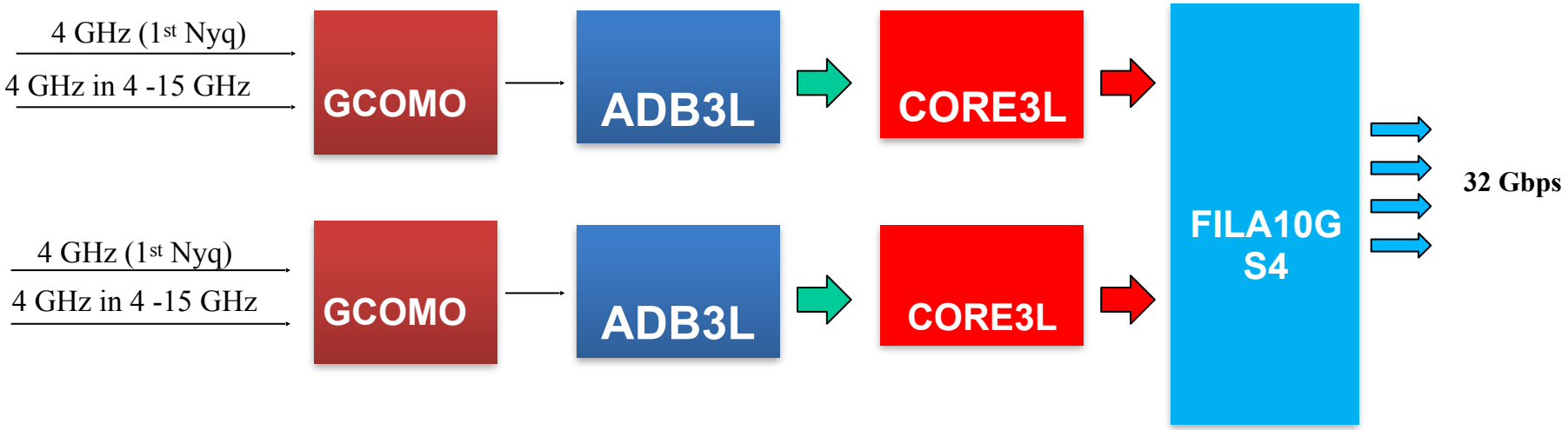


CORE3H

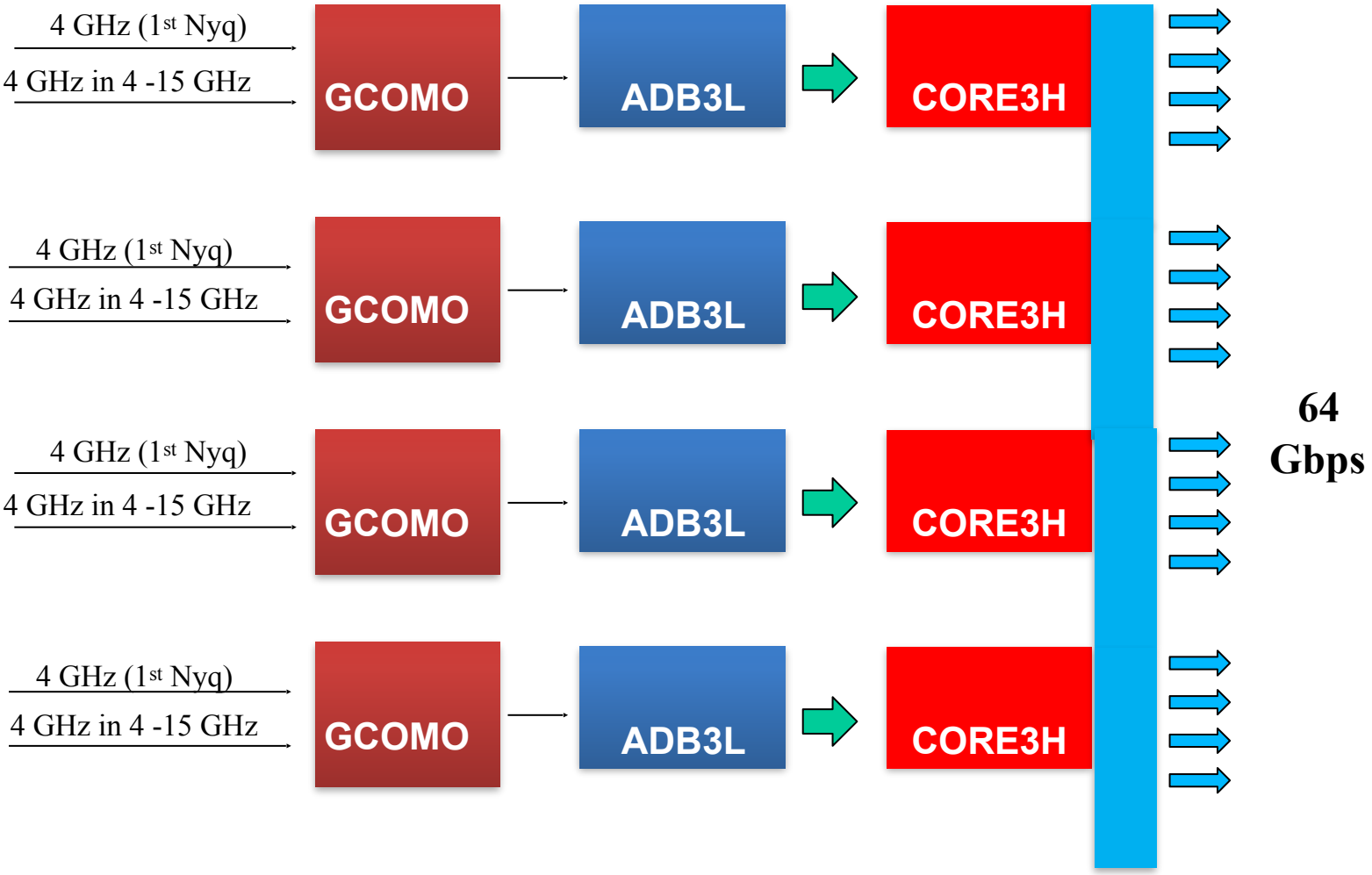


- Input bus: **HSI & HSI2**
- Input sampling representation: **8-10 bit**
- Input bandwidth : 1 x **4GHz, 2 x 2GHz, 4 x 1GHz**
- Processing capability: **DDC, PFB, DCS**
- Output: **8 x 10GE SFP+**
- Inter-board bus: **8 Input 10GE SFP+**
- Compatibility with existing DBBC environment

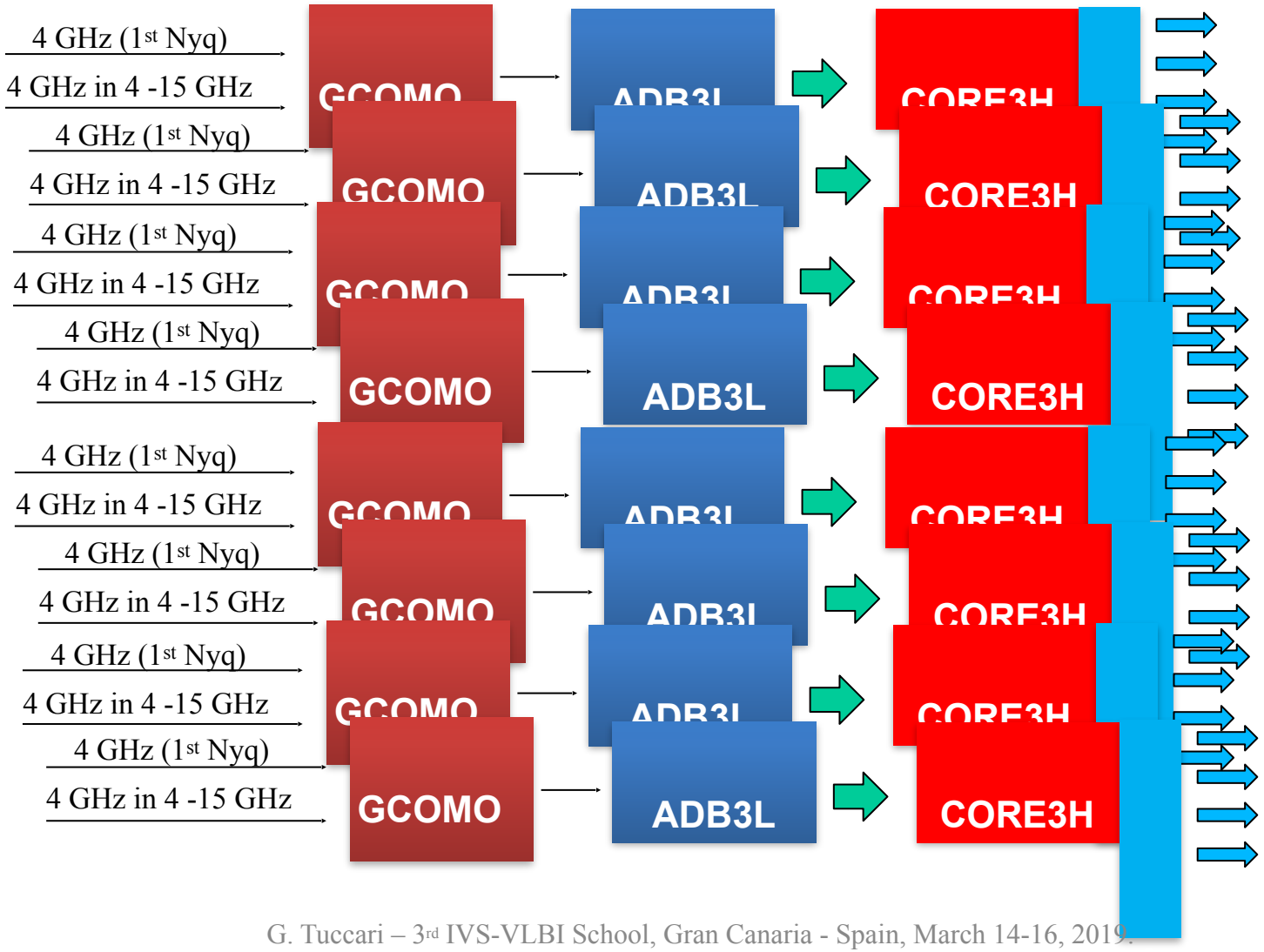
DBBC3L-2L2L Architecture



DBBC3L-4L4H Architecture



DBBC3L-8L8H Architecture

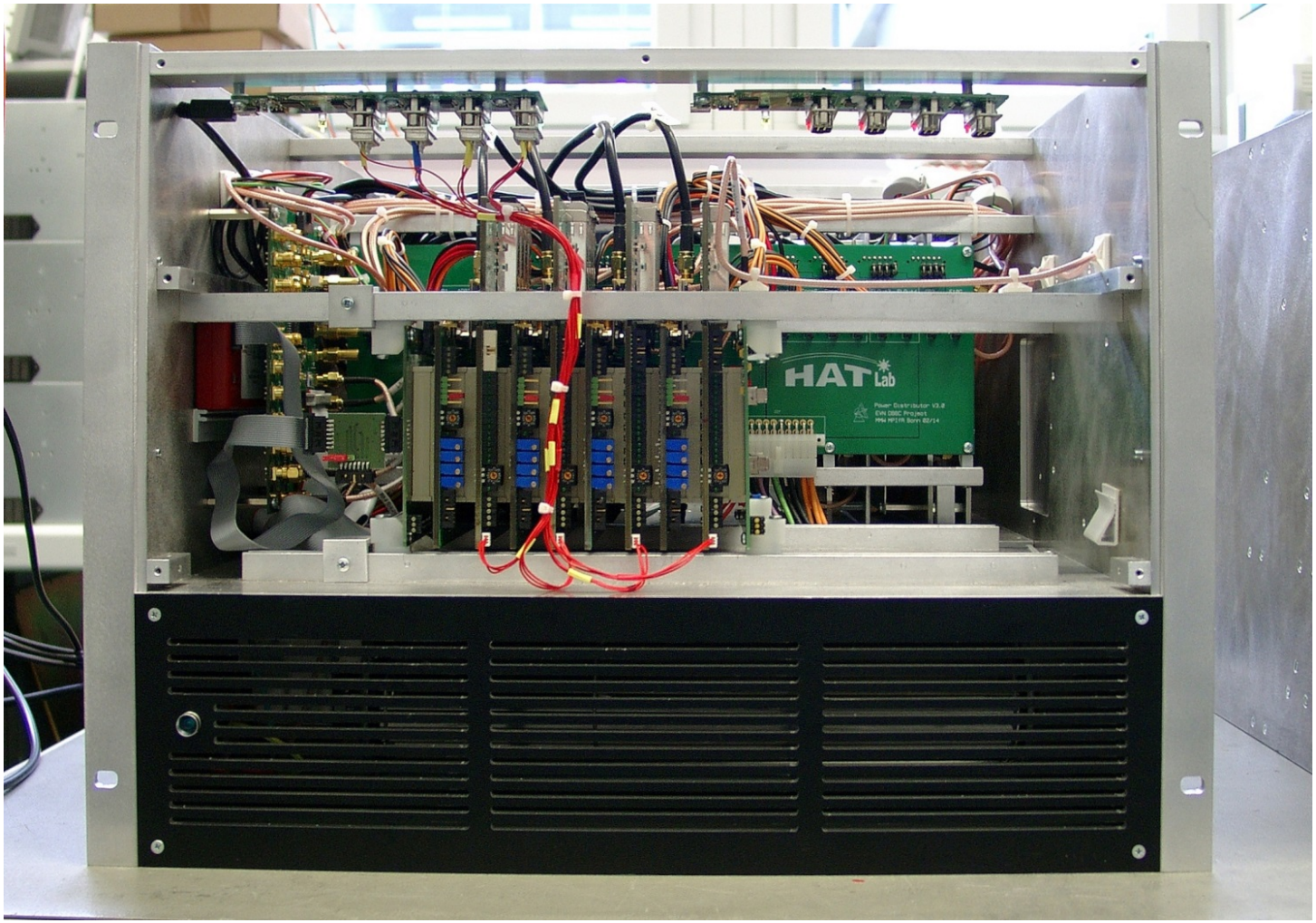


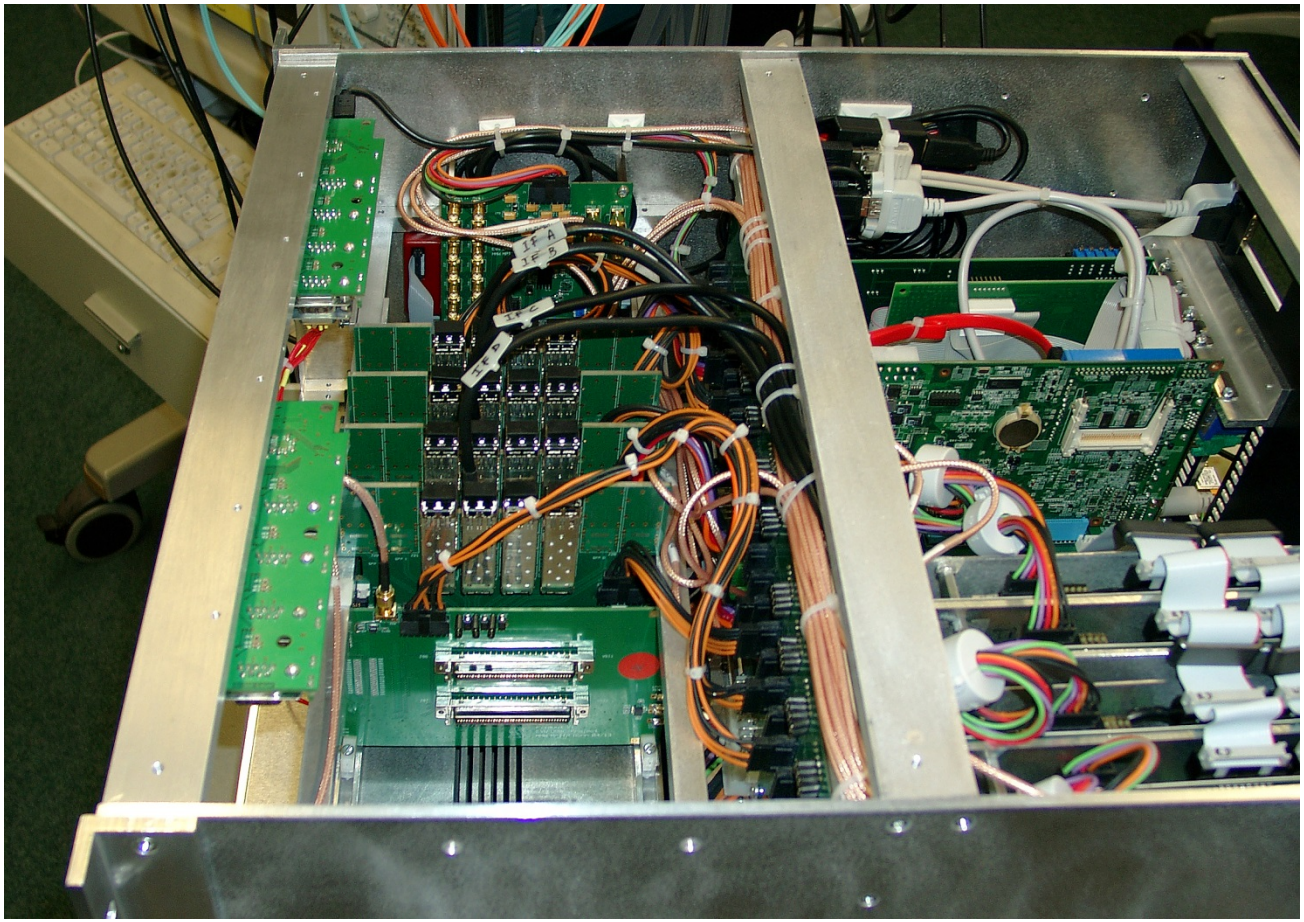
128 Gbps

DBBC3 front view

DBBC3 rear view

DBBC3L
with CORE3H





DBBC3L top view with CORE3H

END of the lecture

Contact me individually or in small groups if you need to have any clarifications, additional information. You will be WELCOME!